

# Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages

## Additional Information

DS1 2012-10

**Edition 2012-10**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

**© 2012 Infineon Technologies AG  
All Rights Reserved.**

#### **LEGAL DISCLAIMER**

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

#### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

## Table of Contents

|          |   |           |
|----------|---|-----------|
| <b>1</b> | <b>Package Description .....</b>        | <b>4</b>  |
| <b>2</b> | <b>Printed Circuit Board (PCB).....</b> | <b>5</b>  |
| 2.1      | Routing.....                            | 5         |
| 2.2      | PCB Pad Design.....                     | 5         |
| <b>3</b> | <b>Board Assembly .....</b>             | <b>6</b>  |
| 3.1      | General Remarks .....                   | 6         |
| 3.2      | Solder Paste.....                       | 6         |
| 3.3      | Solder Stencil .....                    | 6         |
| 3.4      | Component Placement .....               | 6         |
| 3.5      | Reflow Soldering .....                  | 7         |
| <b>4</b> | <b>Cleaning .....</b>                   | <b>9</b>  |
| <b>5</b> | <b>Inspection .....</b>                 | <b>10</b> |
| <b>6</b> | <b>Rework .....</b>                     | <b>12</b> |

### 1 Package Description

Infineon's SG-WLL (Silicon Green - Wafer Level Leadless) packages are bare silicon packages for discrete components with high focus on miniaturization. Those packages are suitable e.g. for applications with limited space on board. For package board interconnection the devices provide a NiP – Pd - Au (Nickel-Phosphorus Palladium Gold) surface on the package pads. The remaining surface besides the pads is covered by silicon nitride.

#### Features

- Smallest x-y-z-package dimensions
- Chip size (silicon)-package without redistribution layer
- MSL1 due to bare silicon product
- No backside protection
- Lead free package
- No package internal interconnect (e.g. wire bond or flip chip connection)



**Figure 1 SG-WLL-2-1 package**

Semiconductor devices are sensitive to excessive electrostatic discharge, moisture, mechanical handling, and contamination. Therefore they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing. For details, please refer to the General Recommendations for Assembly of Infineon Packages in "Package Handling" (available at [www.infineon.com/packages](http://www.infineon.com/packages)).

## **2 Printed Circuit Board (PCB)**

### **2.1 Routing**

PCB design and stack up are key factors for achieving solder joints with high reliability. For example it is known that the board stiffness has a significant influence on the reliability (temperature cycling) of the solder joint interconnect if the application is used in critical temperature cycling conditions. Board stiffness can also be influenced by placement of large components on a double sided assembled PCB.

### **2.2 PCB Pad Design**

The interconnect solder joint-to-board is influenced by:

- General pad technology (Solder Mask Defined; short: SMD and Non Solder Mask Defined; short NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final plating)
- Via layout and technology

Further information can be found in the General Recommendations for Assembly of Infineon Packages by following the links to "Printed Circuit Board" at [www.infineon.com/packages](http://www.infineon.com/packages).

Generally we recommend NSMD pad design for SG-WLL packages. This is based on the fact that those packages and also their connection pads have very small sizes and NSMD design eliminates the influence of PCB manufacturing tolerances of the solder mask layer. On the other hand NSMD design opens parts of the lines connecting the pads to the remaining circuit because the solder mask opening is bigger than the pad itself. To minimize the influence of the solder paste wetting these open parts of the lines during reflow soldering the width of the connecting lines on the PCB should be as small as possible (100µm or less). Depending on the capabilities of the PCB manufacturer it might be not possible to separate two PCB pads of one SG-WLL package by a solder mask dam. Providing that the stencil openings for the solder paste printing process are suitable designed and the printing process itself is well controlled the missing solder mask dam between the pads can be seen as uncritical. Experiments have shown that it is helpful to increase the PCB pad size slightly compared to the package pads. For further information on recommended PCB pad design please contact the Infineon sales representative.

In general assembling SG-WLL packages is similar to the TS(S)LP Infineon package family, both are using bottom located contact pads, some of them are also using very similar or even the same footprint (e.g. PG-TSSLP-2-1, SG-WLL-2-1).

## **3 Board Assembly**

### **3.1 General Remarks**

Many factors within the board assembly process influence assembly yield and board-level reliability. Examples include design and material of the stencil, the solder paste material, solder paste printing process, component placement, and reflow process. We want to emphasize that this document is just a guideline to support our customers in selection of the appropriate processes and materials. Additionally, optimization studies at the customer's own facilities that take into account the actual PCB, the customer's SMT equipment, and product-specific requirements is necessary.

### **3.2 Solder Paste**

Solder paste consists of solder alloy and a flux system. Normally the volume is about 50% alloy and 50% flux and solvents. In term of mass, this means approximately 90 wt% alloy and 10 wt% flux and solvents. The flux system has to remove oxides and contamination from the solder joints during the soldering process. The capacity for removing oxides and contamination is given by the relative activation level.

The contained solvent adjusts the viscosity needed for the solder paste application process. The solvent has to evaporate during reflow soldering.

Pb-free solder pastes typically contain SAC305 (3.0 % Ag and 0.5 % Cu) or other so-called SnAgCu (SAC) alloys (typically 1-4% Ag and <1% Cu).

A "no-clean" solder paste is preferred for SG-WLL packages since the solder joints will be formed below the components where cleaning is difficult or even not possible.

The paste must be suitable for printing the solder stencil aperture dimensions; the usage of paste type 4 or a higher type (with lower grain size of the solder alloy powder) is recommended.

Solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

### **3.3 Solder Stencil**

The solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. Too much solder paste will cause solder bridging, whereas too little solder paste can lead to insufficient solder wetting between all contact surfaces. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For SG-WLL packages a stencil thickness of maximum 100µm is recommended. Depending on the dedicated package the stencil thickness might need to be thinner. Generally it needs to be ensured that the area ratio which describes feasible stencil thicknesses in relation to the aperture sizes used meets the requirements.

To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) are preferred.

For further details and specific stencil aperture recommendations please contact your sales representative.

Please note that the recommendations are only rough guidelines. The most suitable layout for a specific application depends on the factors mentioned in this document.

### **3.4 Component Placement**

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry.

Component placement accuracies of  $\pm 50\text{ }\mu\text{m}$  are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately before the mounting process.

Recognition of the packages is performed by a special vision system, enabling the complete package to be centered correctly. We recommend teaching the package pads to your component vision system, not only the package outline.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB. For SG-WLL packages this means maximum displacement of  $50 - 70\text{ }\mu\text{m}$ .

Additionally it is necessary to select a suitable nozzle for the pick and place process. The nozzle size (outer dimensions) should not exceed the package dimensions. Larger nozzles can lead to pick up errors during removing the components from the tape.

Generally manual placement or handling of SG-WLL packages should be seen as critical since bare silicon devices need to be handled with the right tools and much care. Scrubbing at any side of the components should be avoided.

For details about factors influencing the component placement please refer to the General Recommendations for Assembly of Infineon Packages in "Mounting of SMDs" (available at [www.infineon.com/packages](http://www.infineon.com/packages)).

### 3.5 Reflow Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes such as:

- Forced convection
- Vapor phase
- Infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of the SG-WLL packages.

Wave soldering is not possible. During the reflow process, each solder joint has to be exposed to temperatures above solder melting point (liquidus) for a sufficient time to get the optimum solder-joint quality, whereas overheating the PCB with its components has to be avoided. Because of their size and thickness SG-WLL packages are qualified to withstand a maximum package body temperature of  $260^{\circ}\text{C}$  (this refers to IPC/ JEDEC J-STD-020).

When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components.

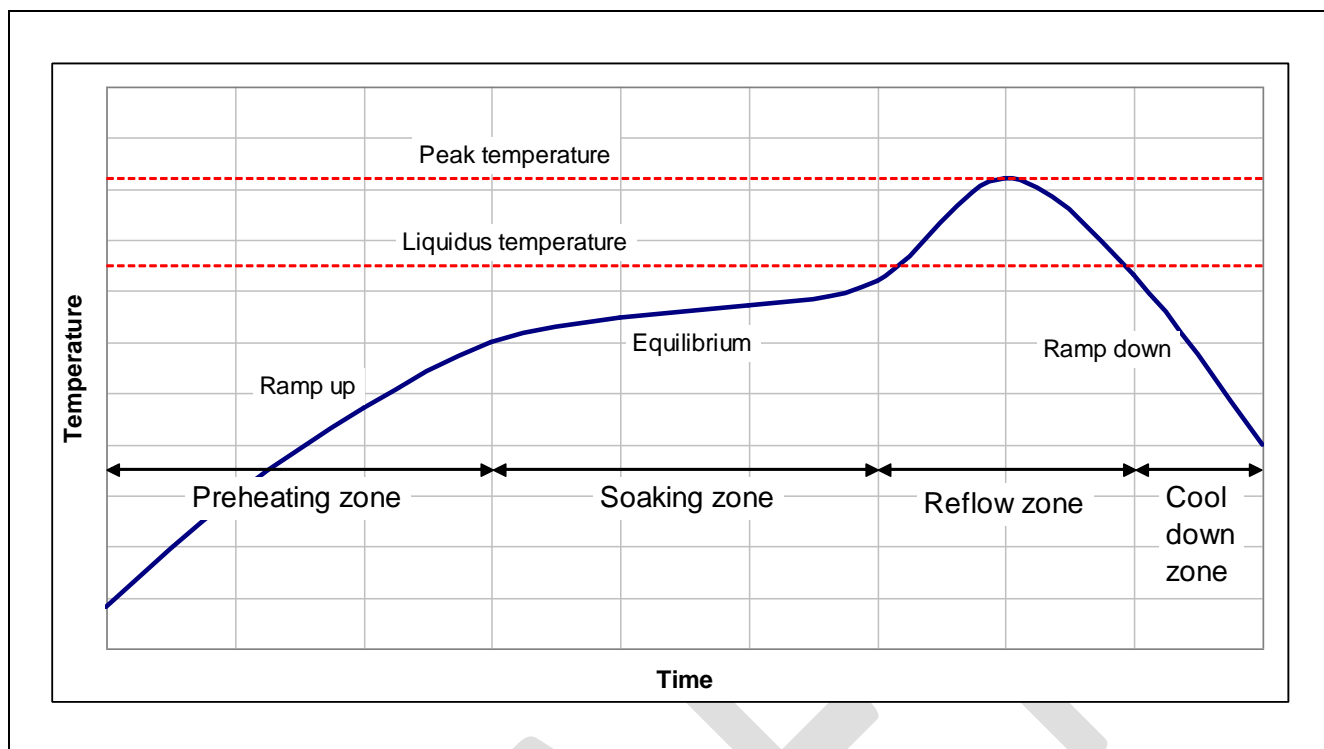
The recommended type of process is forced-convection reflow. Using a nitrogen atmosphere can generally improve solder-joint quality, especially for Pb-free alloys nitrogen may contribute to shiny and oxide-free solder-joints.

Figure 2 shows a general forced-convection reflow profile.

Table Y shows the key data of such a reflow profile, based on the JSTD-020 standard. SG-WLL packages are qualified concerning their resistance to heat according to the maximum temperatures of this table.

SG-WLL packages are generally suitable for double sided mounting as well.

For further details about the reflow profile (especially for Pb-containing solder pastes), please refer to the General Recommendations for Assembly of Infineon Packages in "Mounting of SMDs," available at [www.infineon.com/packages](http://www.infineon.com/packages).



**Figure 2** General forced-convection reflow solder profile

**Table 1** EXAMPLE of the key data for a forced-convection reflow solder profile

| parameter  | minimum value | typical value | max. value<br>(acc. IPC/ JEDEC<br>J-STD020) | main influence                |
|--|---------------|---------------|---|-------------------------------|
| preheating rate                                  | 1.0 K/s       | 2.5 K/s       | 3.0 K/s                                     | flux system<br>(solder paste) |
| soaking temperature                              | 140 – 170 °C  | 140 – 170 °C  | 150 – 200 °C                                | flux system<br>(solder paste) |
| soaking time                                     | 50 s          | 80 s          | 120 s                                       | flux system<br>(solder paste) |
| peak temperature                                 | 230 °C        | 245 °C        | 260 °C                                      | alloy<br>(solder paste)       |
| reflow time above<br>melting point<br>(liquidus) | 40 s          | 60 s          | 150 s                                       | alloy<br>(solder paste)       |
| cool-down rate                                   | 1.0 K/s       | 2.5 K/s       | 8.0 K/s                                     |                               |



## **4 Cleaning**

After the reflow soldering process, some flux residues can be found around the solder joints or spreading over the whole PCB. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. Cleaning beneath a SG-WLL package is difficult because of the solder joints being below the component and the small gap between package and PCB, and is therefore not recommended. If the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and solution have to be selected while taking into account the kinds of packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Even small residues of the cleaning solution should be removed/ dried very thoroughly. Contact the solder paste or flux manufacturer for recommended cleaning solutions.

DRAFT

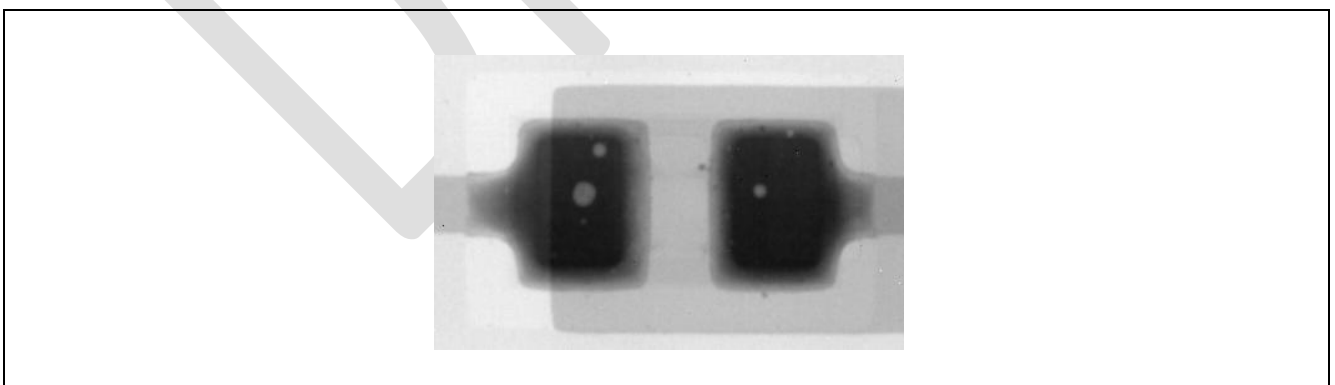
## 5 Inspection

A visual inspection of the solder joints with conventional AOI (Automatic Optical Inspection) systems or a manual visual inspection is limited to the outer surface of the solder joints. In most cases, these are visible and can be judged by looking at them from the side (not from the top like most of the AOI systems). When it comes to SG-WLL packages optical inspections are usually not very successful. Only big misplacement errors and wrong polarity can be checked.



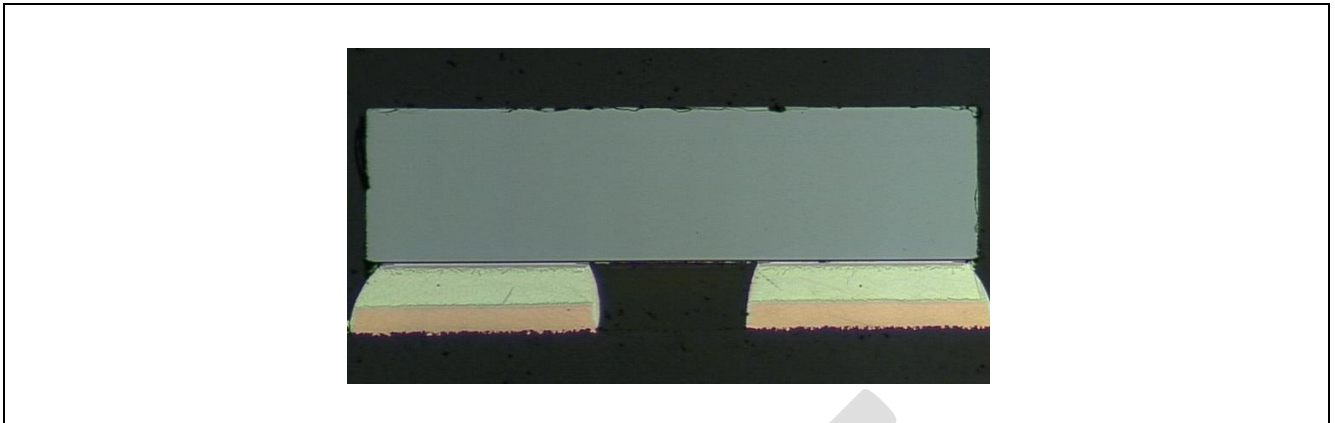
**Figure 3 SG-WLL-2-1 package after reflow soldering**

The only reasonable method for efficient inline control is the implementation of AXI (Automatic X-ray Inspection) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analysing, and data transfer routines. These systems quite reliably enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray. For the acceptability of electronic assemblies, please refer also to the IPC-A-610 standard.



**Figure 4 X-Ray image of a SG-WLL-2-1 package after reflow soldering**

Cross sectioning of a soldered package can serve as tools for sample monitoring or initial process control. They help to get an idea about the quality of the solder joint, intermetallic compounds, and voids.



**Figure 5 Cross section of a SG-WLL-2-1 package after reflow soldering**

Due to the packages being a bare silicon product an inspection after reflow soldering need to be aware that a very small tilt of a package will look more severe than it really is. The shiny backside surface appears different even if the tilt is less than expected to be a defect or affecting the reliability of the solder joints. Especially SG-WLL-2 packages show the described phenomenon due to the fact that 2 pin packages always show a tilt. Investigations on the 2<sup>nd</sup> level reliability have proven that even the tilt of 2 pin packages do not affect the solder joint lifetime.



**Figure 6 SG-WLL-2 packages soldered on board**

## **6 Rework**

If a defective component is detected after board assembly, generally a device can be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused. Nevertheless, desoldering the old component (if analysis afterwards is planned) and resoldering of the new component has to be done very thoroughly.

Repair of single solder joints is not recommended.

Especially for SG-WLL packages you need to take into account that the devices are very small and the device material is bare silicon. If a rework (component replacement) is planned the equipment used should be suitable for smallest package sizes and handling of silicon devices (e.g. no metal tweezers used).

DRAFT

[www.infineon.com](http://www.infineon.com)