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Forward Converter Design Note

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1 Introduction

The single transistor forward converter is commonly used for off-line supplies in the power range below 200W. Its simplicity and low component count makes it a viable alternative to the Flyback, when galvanic isolation and/or voltage step-up/-down is required. The Forward is generally a good choice when high output current is required. This document aims to discuss the Single Ended Forward topology in detail and point out some key differences to Flyback topology. The operational mode and detailed design equations for a typical off-line supply is provided.

2 Forward Converter Topology

Derived from the buck topology, the single transistor forward converter employs a transformer and thus a means of galvanic isolation as well as voltage step-up or step-down, which makes it a good choice for off-line applications requiring both. The single active switch is sufficient at lower power levels below 200W, where component stresses are modest and a half- or full-bridge type topology is not needed.

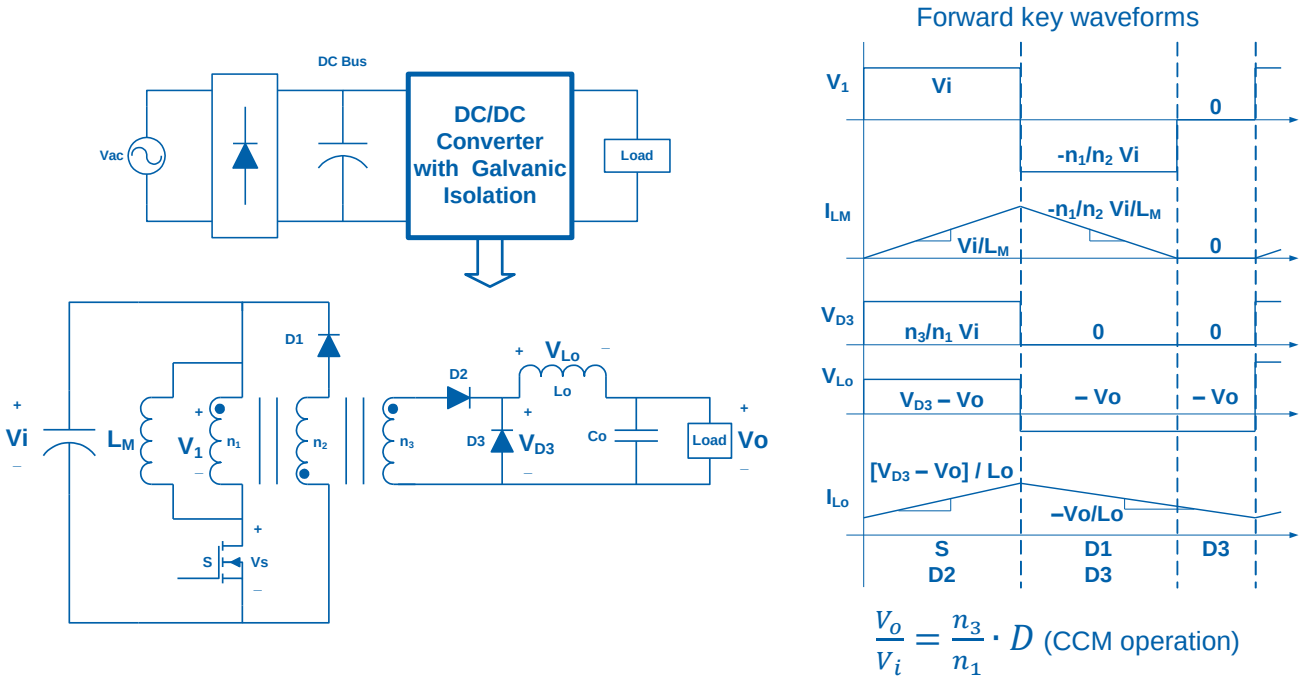

Figure 2.1: Diagram, schematic and basic waveforms for single ended forward converter

2.1 Key advantages over Flyback

The Forward converter looks similar to the Flyback at first glance, but is fundamentally different in its operation and features. The main advantages over the Flyback are:

1. Better transformer utilization: The Forward converter transfers energy instantly across the transformer and does not rely on energy storage in this element. The transformer can thus be made more ideal with much higher magnetizing inductance and no air gap. The resulting lower peak currents in primary as well as secondary means lower copper losses compared to Flyback.
2. Filtered output: the output inductor and freewheeling diode keeps the output current fairly constant and the secondary ripply current is dramatically reduced. Energy storage is mainly in the output inductor, and the output capacitor can be made fairly small with a much lower ripple current rating; its main purpose is to reduce output voltage ripple.
3. Lower active device peak current: due to much larger magnetizing inductance

2.2 Key drawbacks compared to Flyback

The forward converter does have some drawbacks compared to Flyback, which include:

1. Increased cost: Since extra output inductor and freewheeling diode is required
2. Minimum load requirements: particularly with multiple outputs, since gain dramatically changes if converter goes into DCM operation (at light loads).
3. Higher voltage requirement for the MOSFET – which often discourages use in off-line applications that must work on 230V grids.

3 Design Equations

The following are design equations for the single transistor forward converter including a design example to further clarify the use of the equations.

Input voltage {Vi}	130 V-200 Vdc (PFC pre-regulated bus – 110 Vac)
Output voltage {Vo}	3.3 V
Maximum output current {Io,max}	20 A
Maximum power {Po,max}	66 W
Switching frequency {fs}	100 kHz
Minimum load	10 %

Table 3.1: Specifications

3.1 Transformer considerations

The winding ratio between the primary winding, n_1, and the reset winding, n_2, is often chosen as 1 for ease, which will also be the case here. This ratio defines maximum duty raito D≤50% to ensure proper reset.

The winding ratio between the primary winding, n_1, and the secondary winding, n_3, must be small enough to ensure the required output voltage can be achieved at maximum D and minimum Vi, but large enough to use entire D range. For CCM operation the gain is the standard buck gain modified by the winding ratio and can be rearranged to yield the winding ratio at specified operating conditions:

$$\frac{V_o}{V_i} = \frac{n_3}{n_1} \cdot D \quad \Rightarrow \quad \frac{n_1}{n_3} < 15.11 \qquad \textbf{(1)}$$

When V_o is 4.3 V (3.3 V + 1 V extra for assumed voltage drop across D2 and Lo),
Vi is 130 V and
D is 50 %.

One choice of core size could be ETD34, which requires a minimum primary turns-count in order to guarantee non-saturation:

$$n_1 > \frac{Vi_{MAX} \cdot D_{MAX} \cdot \frac{1}{fs}}{B_{sat} \cdot A_e} \quad \Rightarrow \quad n_1 > 34.3\,turns \qquad \textbf{(2)}$$

For Vi_{MAX}=200 V
D_{MAX}=0.5
Fs=$100 \cdot 10^3$ Hz
Bsat=0.3 T (max allowed core flux densitiy for ferrites to guarantee non-saturation) and
Ae=$97.1 \cdot 10^{-6}$ m2 for ETD34

Since a winding ratio n1/n3≤15 is needed and a minimum of 35 turns for n1 in order to avoid saturation, we can chose

n3=3 turns

n1≡n2=45 turns for a n1/n3 ratio of 15

To check whether the turns will theoretically fit in the available window space, we chose AWG#26 (which is appropriate for the skin depth for fs=100kHz) for n1 and n2. For the high (DC) current secondary side, a foil of full width and at least twice the skin depth in thickness should be used. Some layers of tape will also be required for extra primary-secondary isolation mandated by regulatory compliance. The total area required, A_{req}, for all the windings and isolation is verified to fit in the available window space, A_W:

$$A_{req} \approx 81\,mm^2 < A_W = 123\,mm^2 \quad \textbf{(3)}$$

The final considerations for the transformer are the structure of the windings, power losses and thermal capabilities, which will not be addressed in present design note. Experimentation with core sizes, ferrite materials and different construction could yield improvements.

3.2 Output inductor considerations

The output inductor must have an inductance value large enough to ensure CCM at 10% load. There is no theoretic upper limit to the inductance value – however larger value means physically larger part as well as more and longer turns, which increase DCR and thus copper losses.

To calculate the minimum value, we first consider the minimum DC current through the inductor:

$$I_{Lo,DC,\min} = I_{o,\max} \cdot 10\% = 2\ A \quad \textbf{(4)}$$

In order not to reach zero inductor current in this case, the peak-peak ripple must be less than twice this value:

$$\Delta i_{Lo} < 4\ A \quad \textbf{(5)}$$

The peak-peak ripple current on the inductor can be calculated for rising current during the ON-time (when S conducts) or decaying current during the OFF-time (when D3 conducts):

$$\Delta i_{Lo} = \left(\frac{n_3}{n_1} \cdot V_i - V_o \right) \cdot \frac{1}{L_o} \cdot t_{on} \quad \textbf{(6)}$$

Where t_{on} is the ON-period of S

Remembering that the gain is given by

$$\frac{V_o}{V_i} = \frac{n_3}{n_1} \cdot D \quad \underset{D=t_{on} \cdot fs}{\Rightarrow} \quad t_{on} = \frac{V_o}{V_i} \cdot \frac{n_1}{n_3} \cdot \frac{1}{fs} \quad \textbf{(7)}$$

We can substitute (7) into (6):

$$\Delta i_{Lo} = \left(\frac{n_3}{n_1} \cdot V_i - V_o \right) \cdot \frac{1}{L_o} \cdot \frac{V_o}{V_i} \cdot \frac{n_1}{n_3} \cdot \frac{1}{fs} \quad \Rightarrow \quad \Delta i_{Lo} = \left(1 - \frac{1}{V_i} \cdot \frac{n_1}{n_3} \cdot V_o \right) \cdot \frac{1}{L_o} \cdot V_o \cdot \frac{1}{fs} \quad \textbf{(8)}$$

Substituting into (5) yields:

$$\Delta i_{Lo} < 4\ A \quad \Rightarrow \quad L_o > \left(1 - \frac{1}{V_i} \cdot \frac{n_1}{n_3} \cdot V_o \right) \cdot \frac{1}{4\ A} \cdot V_o \cdot \frac{1}{fs} \quad \Rightarrow \quad L_o > 6.2\ \mu H \quad \textbf{(9)}$$

For V_i=200 V and

V_o=3.3 V

The only term not constant in the expression in (9) is V_i which can assume a range of values. It is clear that the highest value that can occur to the right of the unequal sign is when V_i is at its maximum. A value of ~8.5 uH could be chosen to account for inductance tolerance and some voltage drop.

Since the output current seen by the inductor is mostly DC (with “small” AC ripple), the DC resistance is the most critical to determine a majority of the loss contributions. The loss incurred from inductor DCR is straightforward Irms squared times DCR.

3.3 MOSFET considerations

The highest primary side current will occur when full output power is delivered at lowest input voltage. Target efficiency for this converter could be in the range of 75%, which means the average primary side power is

$$\eta = \frac{P_o}{P_i} \quad \Rightarrow \quad P_i = 88\,W \tag{10}$$

D in this scenario was ~0.5 as determined in (1), leading to a mean primary side current during t_{on} of

$$I_{pri,mean,on} = \frac{P_i}{V_i \cdot D} \approx 1.35\ A \tag{11}$$

The ripple on the output inductor is

$$\Delta i_{Lo} = \left(\frac{n_3}{n_1} \cdot V_i - V_o \right) \cdot \frac{1}{L_o} \cdot t_{on} \approx 3.12\ A_{p-p} \quad \Rightarrow \quad \frac{\Delta i_{Lo}}{I_{Lo,\max}} \approx 16\ \% \tag{12}$$

For L_o=8.5 µH

Half of this peak-peak ripple – as a percentage – is present on top of the mean primary current in n1 winding at the end of t_{on}.

$$\Delta i_{pri} = \frac{\Delta i_{Lo}}{2 \cdot I_{Lo,\max}} \cdot I_{pri,mean,on} = 0.11\ A_p \tag{13}$$

The primary winding is in parallel with the magnetizing inductance, and their added currents flow through the primary side switch. The magnetizing current must start from zero at the beginning of each t_{on} period (enforced by the reset-winding), and will reach its peak at the end of t_{on} (just like the n1 current). The peak value is given by

$$\Delta i_{L_M} = V_i \cdot \frac{1}{L_M} \cdot t_{on} = 0.24\ A_{p-p} \tag{14}$$

For V_i=130 V and

L_M=2.7 mH (if transformer built with small air gap on 3C90 ferrite material for ETD34 core)

Which brings the total max peak current seen by the active switch to

$$I_{S,peak} = I_{pri,mean,on} + \Delta i_{pri} + \Delta i_{L_M} = 1.7\ A \tag{15}$$

The rms value of the current flowing through the MOSFET in above scenario can be calculated by

$$I_{S,\max,RMS} = I_{S,mean} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_S}{I_{S,mean}} \right)^2} = 1.05\ A_{rms} \tag{16}$$

Where $I_{S,mean}$=1.5 A (primary mean current plus one-half of peak-peak magnetizing ripple current) and

Δi_S=0.23 A (primary current ripple plus one-half of peak-peak magnetizing ripple current)

The voltage seen by the MOSFET during turn-off must be evaluated, and can be calculated by adding the input and the voltage across n2, transformed by the winding ratio (n1/n2). When D1 is conducting (and assumed ideal), the input voltage exists across the reset winding, n2 and is dot-negative. This voltage will be enforced by the transformer to exist across the primary winding, n1 – also dot-negative – modified by the winding ratio. Due to the polarity of the dots, the voltage across S is thus

$$V_S = V_i + \frac{n_1}{n_2} \cdot V_i = 400\,V \quad \textbf{(17)}$$

The leakage inductance of the transformer wil cause additional ringing across S. Allowing for 10% overshoot caused by the transformer leakage inductance and additional 20% derating, the MOSFET selected must have a voltage rating of at least

$$V_{S,br,\min} = 528\,V \quad \textbf{(18)}$$

Besides ample voltage- and current –ratings, there are other selection criteria to consider when chosing the MOSFET:

- Low FOMs – R_{on}*Q_g and R_{on}*Q_{oss}
- Fast turn-off switching – high gate plateau
- Low E_{oss}, since this is dissipated in R_{on} during turn-on
- Switching and condution losses should be fairly balanced for minimum total losses – typically optimized at full output power and low input voltage (worst-case thermally)

The conduction losses can directly be found after MOSFET has been selected:

$$P_{S,cond} = I_{S,\max,RMS}^{\ 2} \cdot R_{on(100°C)}\ W \quad \textbf{(19)}$$

By turning on, the MOSFET takes over the output inductor current – reflected through the transformer – from D3. The transition happens in two stages. During stage 1 the current in the D3 commutates to D2; and through the transformer primary winding rises from zero to its final value through the MOSFET. During stage 2, when the current has fully commutated, the voltage will fall across the MOSFET d-s until the MOSFET has fully turned on and its d-s voltage is approximately zero. The instantaneous power dissipated in the MOSFET during the transition forms a triangle with a peak amplitude equal to the product of the commutating current amplitude and the initial drain-source voltage. The base of the triangle has a total length equal to the sum of the time durations of stage 1 and stage 2. We already know V_i and can easily calculate $I_{S,0}$:

$$I_{S,0} = I_{pri,mean,on} - \Delta i_{pri} = 1.25\ A \quad \textbf{(20)}$$

Time duration of stage 1 is determined by the driver charging the MOSFET input capacitance from V_{th} to V_{pl}:

$$t_{on,1} = C_{iss} \cdot R_g \cdot \left(\ln\left[-\frac{V_{th} - V_{drv}}{V_{drv}} \right] - \ln\left[1 - \frac{V_{pl}}{V_{drv}} \right] \right) \quad \textbf{(21)}$$

Time duration of stage 2 is determined by the driver dis-charging the MOSFET reverse transfer capacitance from V_S (less V_{pl}) to zero

$$t_{on,2} = -\frac{C_{rss} \cdot R_g \cdot \left(V_i - V_{pl} \right)}{V_{pl} - V_{drv}} \quad \textbf{(22)}$$

The total turn-on losses can now be found:

$$P_{S,turn-on} = \frac{1}{2} \cdot \left(t_{on,1} + t_{on,2} \right) \cdot I_{S,0} \cdot V_i \cdot fs \quad \textbf{(23)}$$

When turning off, the MOSFET has to swing twice the input voltage (due to the reset action), and it's peak current. During stage 1 the voltage transitions, while the MOSFET is going through the Miller region, where the driver must charge the reverse transfer capacitance to twice the input voltage (less V_{pl})

$$t_{off,1} = -\frac{C_{rss} \cdot R_g \cdot \left(V_{pl} - 2 \cdot V_i \right)}{V_{pl}} \quad \textbf{(24)}$$

During stage 2 the current commutates while the driver discharges C_{iss} from V_{pl} to V_{th}

$$t_{off,2} = R_g \cdot C_{iss} \cdot \ln\left(\frac{V_{pl} - 0}{V_{th} - 0}\right) \quad \textbf{(25)}$$

The total turn-off loss is then

$$P_{S,turn-off} = \frac{1}{2} \cdot \left(t_{off,1} + t_{off,2}\right) \cdot I_{S,peak} \cdot 2 \cdot V_i \cdot fs \quad \textbf{(26)}$$

The MOSFET output capacitance, C_{oss}, holds a charge before turn-on, which is dissipated in the MOSFET during turn-on. The associated switching loss is calculated by

$$P_{S,oss} = E_{oss} \cdot fs \quad \textbf{(27)}$$

Finally there is the driver loss associated with charging and discharging the gate charge

$$P_{S,drv} = V_{drv} \cdot Q_g \cdot fs \quad \textbf{(28)}$$

The total dynamic loss is the sum of the turn-on, turn-off, E_{oss} and driver losses. The total dynamic loss should be similar as the conduction loss at high output power and low input voltage. For this design, one recommendation could be **IPA60R280E6**. This MOSFET has a sufficient current rating of 8.7A and a sufficient voltage rating of 600V. The total dynamic loss comes out to

0.51 W and the conduction loss is

0.49 W at full output power and minimum input voltage if 15Ω gate resistor and a 12V driver is used.

The package is already fully electrically isolated (FullPAK), and can be directly bolted onto an appropriate heat sink.

3.4 Diode considerations

There are three diodes in the application. D1 will recover softly, when the magnetizing inductance is fully discharged, and the current seen by the diode is fairly modest under most circumstances. The highest current is experienced during startup or transients, when max duty cycle (D=0.5) can occur at highest input voltage (V_i=200 V).

$$I_{D1,\max,RMS} = \frac{V_{i\max}}{L_M} \cdot \frac{1}{D_{MAX}} \cdot \sqrt{\frac{fs}{3}} = 0.22\ A_{rms} \quad \textbf{(29)}$$

The diode loss is highest under these circumstances:

$$P_{D1} = I_{D1,\max,RMS} \cdot V_F \quad \textbf{(30)}$$

D1 must withstand a maximum reverse voltage of

$$V_{D1,MAX} = \frac{n_2}{n_1} \cdot V_{i,\max} \cdot 1.1 \cdot 1.2 = 264\,V \quad \textbf{(31)}$$

Allowing for 10% ringing and additional 20% for derating. A power diode with low forward drop, at least twice the max RMS current rating and sufficient voltage rating should be chosen. The reverse recovery characteristics of the diode are not significant.

The minimum reverse voltage rating for D2 and D3 is

$$V_{r,D2,D3} > \left(V_{i\max} \cdot \frac{n_3}{n_2} - V_F \right) \cdot 1.1 \cdot 1.2 = 20\,V \quad \textbf{(32)}$$

When accounting for 25% ringing and 20% derating, and

V_F=0 V (worst case forward voltage drop of the complementary diode)

Each of the secondary side diodes carry roughly the output current during their conduction interval since the ripple is small. Since the on-time is equal for the two secondary side diodes during full power operation – if input voltage is at its minimum – they will have same RMS current, which is worst-case for D2:

$$I_{Lo,RMS} = \sqrt{I_{D2,RMS}{}^2 + I_{D3,RMS}{}^2} \Rightarrow I_{D2,RMS} \equiv I_{D3,RMS} = \frac{I_{Lo,RMS}}{\sqrt{2}} = 14.16\ A_{rms} \quad \textbf{(33)}$$

For D3 the worst-case RMS current occurs at full output power, but maximum input voltage

$$I_{D3,RMS} = I_{Lo,RMS} \cdot \sqrt{1 - \frac{(0.5 + V_o)}{V_{i,\max}} \cdot \frac{n_1}{n_3}} = 17\ A_{rms} \quad \textbf{(34)}$$

Where the expression under the root is 1-D for maximum input voltage and 0.5 V voltage drop across secondary side elements. The diode must be rated to carry the max RMS current.

The combined conduction loss for both diodes, when producing full output power at minimum input voltage is thus

$$P_{D2+D3,cond} \approx I_{Lo,RMS} \cdot V_F\ W \quad \textbf{(35)}$$

Assuming equal V_F forward voltage drop for both diodes.

If Schottky diodes are used, which is reasonable for the required voltage rating found in (32), the switching loss is expressed in terms of depletion-region capacitance:

$$P_{D2,Sw} = \frac{1}{2} \cdot C_{j,D2} \cdot \left(\frac{n_3}{n_2} \cdot V_i \right)^2 \cdot fs\ W \quad \textbf{(36)}$$

And conversely for D3:

$$P_{D3,Sw} = \frac{1}{2} \cdot C_{j,D3} \cdot \left(\frac{n_3}{n_1} \cdot V_i \right)^2 \cdot fs\ W \quad \textbf{(37)}$$

For this application it is possible to find Schottky diodes meeting the required voltage- and current ratings.

4 References

[1] Populate