

Advanced Power Management IC with On-Demand-Power™

Features

- ◆ Configurable On-Demand Power™ algorithm to adaptively scale regulated output voltage in correlation with monitored system activity
- ◆ System sensory interface to monitor activity and demand for regulated voltage domains
- ◆ Constant-on-time, voltage feed-forward, synchronous step-down PWM controller
- ◆ Wide input voltage range: 6.5V to 24V
- ◆ Programmable output voltage range: 3V to 5V
- ◆ PWM and light-load operation
- ◆ Temperature compensated $R_{DS(ON)}$ current sensing
- ◆ Internal softstart
- ◆ Output over and under voltage protection
- ◆ Built-in output discharge circuit
- ◆ SMBUS Interface
- ◆ 5x5mm 40-pin QFN package

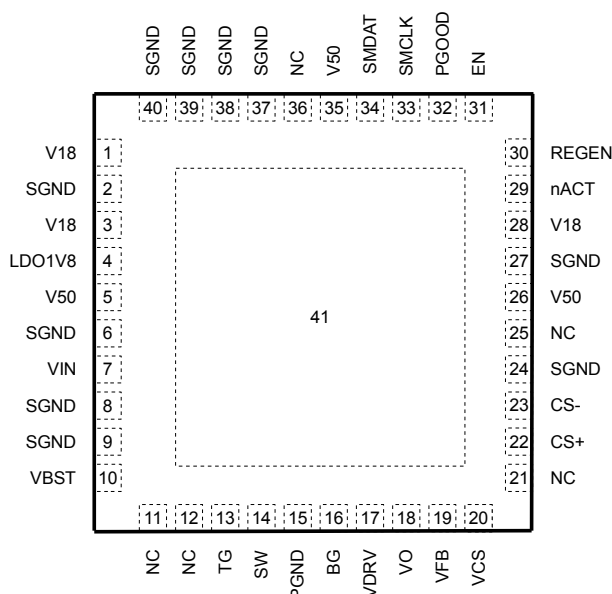
Description

The PSG5210 is a highly integrated power management IC with a synchronous step-down PWM controller for SATA drive power management in mobile computers as well as power management in embedded system applications. Interfaces for monitoring activity, coupled with advanced On-Demand Power algorithms, enable the regulated output voltage of the integrated switching regulator to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution.

Applications

- ◆ Mobile Computers
- ◆ Ultra-Mobile PCs
- ◆ Portable Media Players
- ◆ Other Mobile Devices
- ◆ SATA drives

Pin Configuration



40-LEAD (5mm x 5mm) PLASTIC QFN
EXPOSED PAD (PIN 41) IS SGND. MUST BE SOLDERED TO PCB.

Absolute Maximum Ratings (Note 1)

PARAMETER	VALUE	UNIT
V50 to SGND	-0.3 to 6	V
VDRV to PGND	-0.3 to 6	V
V18 to SGND	-0.3 to 2.0	V
VDDIO to SGND	-0.3 to 6.0	V
VIN to SGND	-0.3 to 30	V
LDO18 to SGND	-0.3 to 2.0	V
VCS to SGND	-0.3 to 6	V
VO, CS+, and CS- to VCS	0.3	V
VO, CS+, and CS- to SGND	-0.3 to 6	V
FB to SGND	-0.3 to 2.0	V
VBST to PGND	-0.3 to 30	V
VBST to SW	-0.3 to 6	V
SW to PGND	-2 to 30	V
BG to PGND	-0.3 to 6	V
BG to VDRV	0.3	V
TG to PGND	-2 to 30	V
TG to SW	-0.3 to 6	V
TG to VBST	0.3	V
All other pins to SGND	-0.3 to 6.0	V
All other pins to VDDIO	0.3	V
Maximum Junction Temperature	125	°C

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Electrical Characteristics

Unless otherwise noted: $V_{IN} = 15V$, $V_{V50} = V_{VDRV} = V_{VDDIO} = 5V$, $V_{V18} = 1.8V$, $V_{SGND} = V_{PGND} = 0V$, $V_{EN} = V_{REGEN} = 5V$, $V_{SMBDAT} = V_{SMBCLK} = 5V$, $V_{nACT} = 5V$, $V_{PGOOD} = 5V$, LDO18 = No Load, $T_A = 0^{\circ}C$ to $70^{\circ}C$. Typical values are at $T_A = 25^{\circ}C$.

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		6.5		24	V
V_{V18}	Digital and analog supply voltage		1.62	1.8	1.98	V
V_{VDDIO}	Digital IO supply voltage		4.5	5	5.5	V
V_{V50}	Analog supply voltage		4.5	5	5.5	V
V_{VDRV}	Bottom gate drive supply voltage		4.5	5	5.5	V
V_{TGDRV}	Top gate drive supply voltage	$V_{TGDRV} = V_{VBST} - V_{SW}$	4.5	5	5.5	V
V_{VCS}	Differential amplifier supply voltage		4.0	5	5.5	V
T_J	Operating junction temperature		0		70	$^{\circ}C$

Power Supplies

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
I_{V18}	Digital and analog supply current Enabled Disabled	$V_{EN} = V_{REGEN} = 5V$ $V_{EN} = V_{REGEN} = 0V$			1.7 28	mA μA
I_{VDDIO}	Digital IO supply current	No switching outputs			25	μA
I_{V50}	Analog supply current Enabled Disabled	No load on LDO18 output $V_{EN} = V_{REGEN} = 5V$ $V_{EN} = V_{REGEN} = 0V$			1.6 48	mA μA
I_{VDRV}	Bottom gate driver supply current Enabled Disabled	All gate drivers are output low $V_{EN} = V_{REGEN} = 5V$ $V_{EN} = V_{REGEN} = 0V$			250 34	μA μA
I_{VBST}	Top gate driver supply current Enabled Disabled	All gate drivers are output low. $V_{EN} = V_{REGEN} = 5V$ $V_{EN} = V_{REGEN} = 0V$			300 150	μA μA
I_{VCS}	Differential amplifier supply current Enabled	$V_{EN} = V_{REGEN} = 5V$, $V_{VCS} = V_{CS+} = V_{CS-} = 5V$			80	μA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
SMBDAT, SMBCLK Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			-5	μA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			5	μA
nACT1, nACT2 Inputs						
V_{IH}	Input high voltage				1.4	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			-10	μA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			10	μA
EN, REG1EN, REG2EN Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			-10	μA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
SMBDAT Output						
V _{OL}	Low level output voltage	I _{OL} = 2mA			0.4	V
I _{OH}	High level output leakage current	Output Voltage = 5V			5	μA
PGOOD Output						
V _{OL}	Low level output voltage	I _{OL} = 2mA			0.4	V
I _{OH}	High level output leakage current	Output Voltage = 5V			10	μA

SMBus Interface (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
f _{SMB}	SMBus clock frequency		10		100	kHz
t _{LOW}	SMBus clock low time	Measured from V _{IL(MAX)} to V _{IL(MAX)}	4.7			μs
t _{HIGH}	SMBus clock high time	Measure from V _{IH(MIN)} to V _{IH(MIN)}	4.0			μs
t _{r,SMB}	SMBus rise time	(Note 4)			1	μs
t _{f,SMB}	SMBus fall time	(Note 5)			0.3	μs
t _{OF}	Output fall time	C _L = 400 pF, I _O = 3mA, (Note 5)			250	ns
t _{TIMEOUT}	SMBDAT and SMBCLK time low for reset of SMBus	(Note 6)	25		35	ms
t _{SU,DAT}	Data setup time		250			ns
t _{HD,DAT}	Data hold time		300			ns
t _{HD,STA}	Hold time after (repeated) start condition. After this period, the first clock is generated.		4			μs
t _{SU,STO}	Stop condition setup time		4			μs
t _{SU,STA}	Repeated start condition setup time		4.7			μs
t _{BUF}	Bus free time between stop and start conditions		4.7			μs

5MHz Internal Oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
f _{5MHZ}	Internal oscillator frequency		4.5		5.5	MHz

Switching Regulators

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
Gate Drivers						
R _{TG(UP)}	TG driver pull-up on resistance	TG high		2.1	8	Ω
R _{TG(DOWN)}	TG driver pull-down on resistance	TG low		1.5	4	Ω
R _{BG(UP)}	BG driver pull-up on resistance	BG high		1.4	8	Ω
R _{BG(DOWN)}	BG driver pull-down on resistance	BG low		0.7	4	Ω
t _{DEAD(TG/BG)}	Dead time	TG low to BG high (Note 7)		53		ns
t _{DEAD(BG/TG)}	Dead time	BG low to TG high (Note 7)		30		ns
V_{OUT} Discharge						
I _{DISCHG}	V _{OUT} discharge current	V _{EN} = 5V, V _{REGEN} = 0V, V _{VOX} = 0.5V	10			mA
Duty and Frequency Control						
t _{ON(1)}	On time	V _{VIN} = 20V, VSETx[7:0] = 55h		389		ns
t _{ON(2)}	On time	V _{VIN} = 20V, VSETx[7:0] = 00h		410		ns
t _{ON(3)}	On time	V _{VIN} = 15V, VSETx[7:0] = 55h		552		ns
t _{ON(4)}	On time	V _{VIN} = 15V, VSETx[7:0] = 00h		616		ns
t _{ON(5)}	On time	V _{VIN} = 10V, VSETx[7:0] = 55h		979		ns

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
$t_{ON(6)}$	On time	$V_{VIN} = 10V$, $VSETx[7:0] = 00h$		1195		ns
$t_{OFF(MIN)}$	Minimum off time			420		ns
$t_{DEAD(MAX)}$	DCM timeout			1026	1130	ns
Softstart						
$t_{SS(10)}$	Softstart time		1.2		2.5	ms
Powergood (PG)						
$V_{PG(L)}$ $V_{PG(H)}$	PG trip voltage Lower PG trip voltage Upper PG trip voltage	With respect to set regulated voltage $V_{VO} = 4V$ to $5V$ V_{VO} ramping negative V_{VO} ramping positive	-600 300		-300 600	mV mV
t_{PGDEL}	PG delay	Entering PG window	115	130	145	μs
Over Voltage Protection (OVP)						
$V_{OVP(F)}$	Fixed OVP trip voltage		5.6		5.9	V
$V_{OVP(D)}$	Dynamic OVP trip voltage	With respect to set regulated voltage $V_{VO} = 4V$ to $5V$	0.8		1.4	V
t_{OVPDEL}	OVP prop delay			10		μs
Under Voltage Protection (UVP)						
V_{UVP}	UVP trip voltage		1.08		1.32	V
t_{UVPDEL}	UVP prop delay		25		40	μs
t_{UVPEN}	UVP enable delay	From rising edge of REGEN	1.9		3.8	ms
Current Sense						
$V_{OCP(OFF)(6)}$	Over current protection offset voltage	OCPROG[3:0]=6h		33		mV
$TC_{OCP(6)}$	Over current protection temperature coefficient	OCPROG[3:0]=6h		118		$\mu V/^{\circ}C$
$V_{OCP(OFF)(8)}$	Over current protection offset voltage	OCPROG[3:0]=8h		41		mV
$TC_{OCP(8)}$	Over current protection temperature coefficient	OCPROG[3:0]=8h		147		$\mu V/^{\circ}C$
$V_{OCP(OFF)(A)}$	Over current protection offset voltage	OCPROG[3:0]=Ah		50		mV
$TC_{OCP(A)}$	Over current protection temperature coefficient	OCPROG[3:0]=Ah		187		$\mu V/^{\circ}C$
$V_{OCP(OFF)(C)}$	Over current protection offset voltage	OCPROG[3:0]=Ch		59		mV
$TC_{OCP(C)}$	Over current protection temperature coefficient	OCPROG[3:0]=Ch		229		$\mu V/^{\circ}C$
V_{ZC}	Zero cross detection comparator offset		-5		8	mV
Programmable Output Voltage						
$V_{PROG(MAX)}$	Maximum programmable output voltage		4.8			V
$V_{PROG(MIN)}$	Minimum programmable output voltage				4	V
$V_{PROG(ERROR)}$	Programmable output voltage error	$VSET[7:0] = 00h$ to $55h$, $V50 = 4.5V$ to $5.5V$, $V18 = 1.62V$ to $1.98V$		14.95	120	mV

1.8V Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
V_{LDO18}	1.8V LDO output voltage	$0 < I_{LDO18} < 5mA$	1.71		1.98	V

Current Sense

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
t_p	Propagation delay	$V_{CS+} - V_{CS-} = 10\text{mV to } 90\text{mV}$, $ITRIP = 50\text{mV}$, $V_{VCS} = 5\text{V}$			10	μs
I_{CS+}	CS+ input bias current	$V_{VCS} = 5\text{V}$, $V_{CS+} = 5\text{V}$, $V_{CS-} = 4\text{V to } 5\text{V}$			120	nA
I_{CS-}	CS- input bias current	$V_{VCS} = 5\text{V}$, $V_{CS+} = 5\text{V}$, $V_{CS-} = 4\text{V to } 5\text{V}$			10	μA
$V_{TRIP(MAX)}$	Maximum programmable trip voltage		90			mV
$V_{TRIP(MIN)}$	Minimum programmable trip voltage				10	mV
$V_{TRIP(ERROR)}$	Programmable trip voltage error	$ISET[7:0] = 00\text{h to } CD\text{h}$, $V50 = 4.5\text{V to } 5.5\text{V}$, $V_{VO} = 4\text{V to } 5.3\text{V}$		0.5	6.25	mV
$V_{TRIP(DRIFT)}$		$ISET[7:0] = 00\text{h to } CD\text{h}$, $V50 = 4.5\text{V to } 5.5\text{V}$, $V_{VO} = 4\text{V to } 5.3\text{V}$		1.71	5	mV

Note 2 Parts are tested at 25°C. Temperature limits established by characterization and are not production tested.

Note 3 Unless otherwise noted, these specifications apply for load capacitances on SMBus lines = 80pF. The switching characteristics of the PSG5220 fully meet or exceed the published specifications of the SMBus version 2.0.

Note 4 The rise time is measured from $(V_{IL(MAX)} - 0.15\text{V})$ to $(V_{IH(MIN)} + 0.15\text{V})$.

Note 5 The fall time is measured from $(V_{IH(MIN)} + 0.15\text{V})$ to $(V_{IL(MAX)} - 0.15\text{V})$.

Note 6 Exceeding $t_{TIMEOUT}$ will reset the PSG5220 SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

Note 7 Delay times are measured using 50% levels.

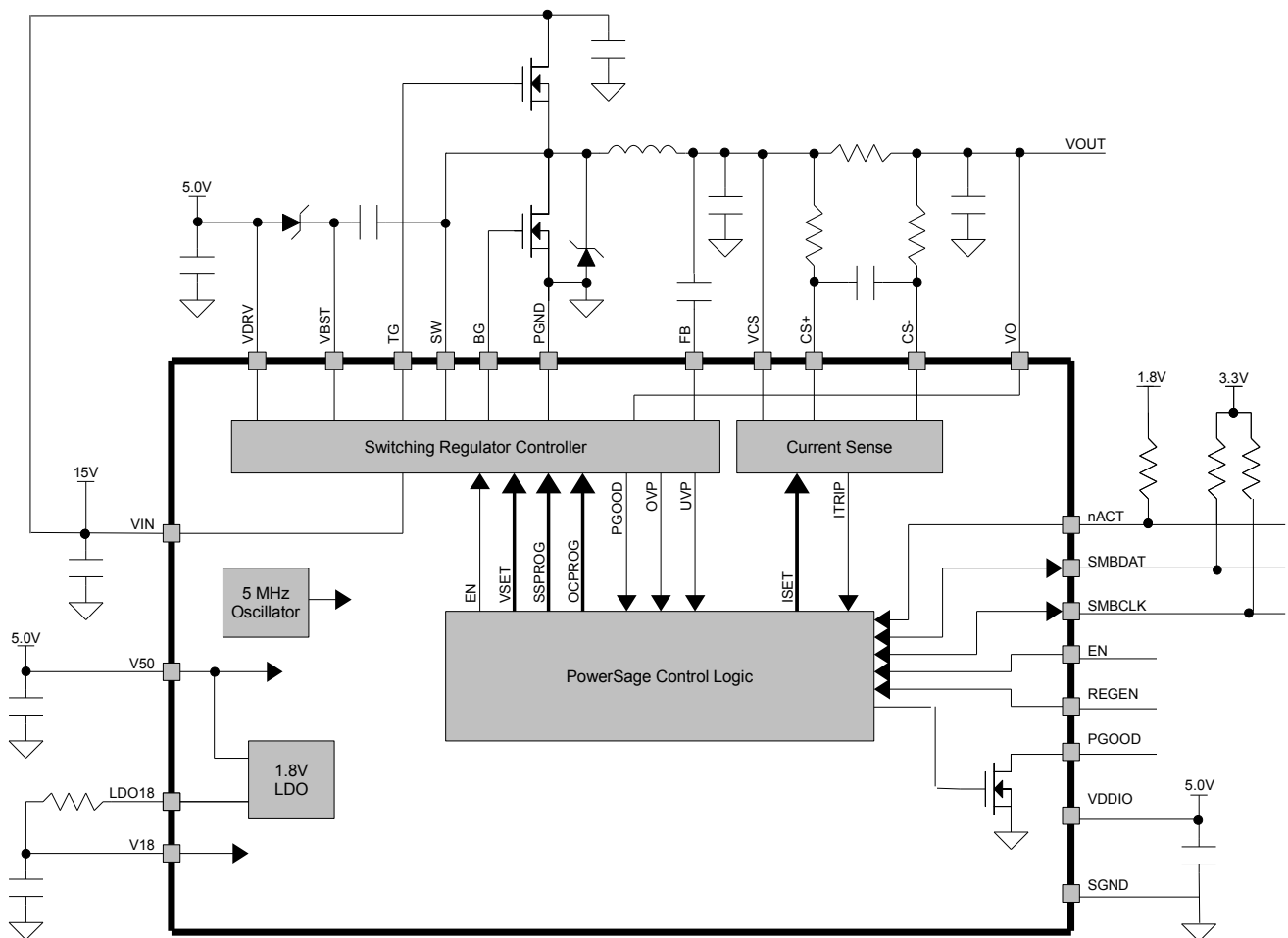
Note 8 Guaranteed by design.

Pin Functions

NAME	PIN	IO (Note 9)	DESCRIPTION
V18	2, 3, 28	P	1.8V power supply for both digital and analog circuitry. Decouple each pin to SGND with a capacitor.
VDDIO	35	P	IO power supply. Decouple to SGND with a capacitor. This is the input supply for digital IO drivers and receivers.
V50	5, 26	P	5V power supply for analog circuitry. Decouple each pin to SGND with a capacitor.
VIN	7	P	High voltage sense input. Decouple to SGND with a capacitor.
SGND	1, 6, 8, 9, 24, 27, 37-40, 41	P	Small signal ground. All small signal components should connect to this ground. Connect SGND to PGND at one point. Pin 41 is the exposed pad
PGND	13	P	Regulator ower grounds. Connect these closely to the appropriate sources of the bottom external N-channel MOSFET and the negative terminal of the VDRV decoupling capacitors. Connect PGND to SGND at one point.
VDRV	15	P	Bottom gate driver supply. Decouple to its respective PGND with a capacitor.
LDO18	4	PO	Internal 1.8V linear regulator output. Decouple to SGND with a series connected resistor and capacitor. This output can be connected to V18 as the 1.8V supply.
VCS	18	P	Differential amplifier supply voltage. Typically connected to the load side of the power inductor. Decouple to SGND with a capacitor.
CS+	22	A	Current sense differential amplifier input. The positive input to the amplifier is normally connected to current sensing resistors through an RC filter.
CS-	23	A	Current sense differential amplifier input. The negative input to the amplifier are normally connected to current sensing resistors through an RC filter.
VO	16	A	Output voltage remote sense inputs.
FB	17	A	Output voltage feedback. Connection point for external ripple injection circuitry or leave floating.
nACT	29	I	Acvity inputs. A logic low indicates that the respective load is active. A logic high indicates that the respective load is idle. Connect directly to VDDIO if not used. Do not leave floating.
SMDAT	34	IOD	SMBus data input/output. The PSG5220 is configured as an SMBus device.
SMCLK	33	IOD	SMBus clock input. The PSG5220 is configured as an SMBus device.
PGOOD	32	OD	Power good indicator output. This open-drain output is pulled to ground when either the channel 1 or channel 2 regulated output voltages leave the regulation window. Each regulator has a fixed 512us power good delay. Each channel has an additional programmable delay and mask.
EN	31	I	Enable input. A logic low disables the switching regulator and forces the PSG5220 into a low-power standby mode. A logic high enables the PSG5220 and the regulator operation is dependent on the REGEN input. Connect directly to VDDIO if not used. Do not leave this pin floating. The output discharge circuit is disabled when EN is a logic low.
REGEN	30	I	Regulator enable input. A logic low disables the switching regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the regulator is dependent on the internal regulator enable bit. Connect directly to VDDIO if not used. Do not leave this pin floating.
VBST	10	P	Boosted floating driver supplies for the top gate driver.
SW	12	A	Switch node connections to power inductors.
TG	11	AO	Top gate driver output.
BG	14	AO	Bottom gate driver output.
NC	19, 20, 21, 25, 36	X	No Connect. These pins should be left floating.

Note 9 P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, X = Unconnected

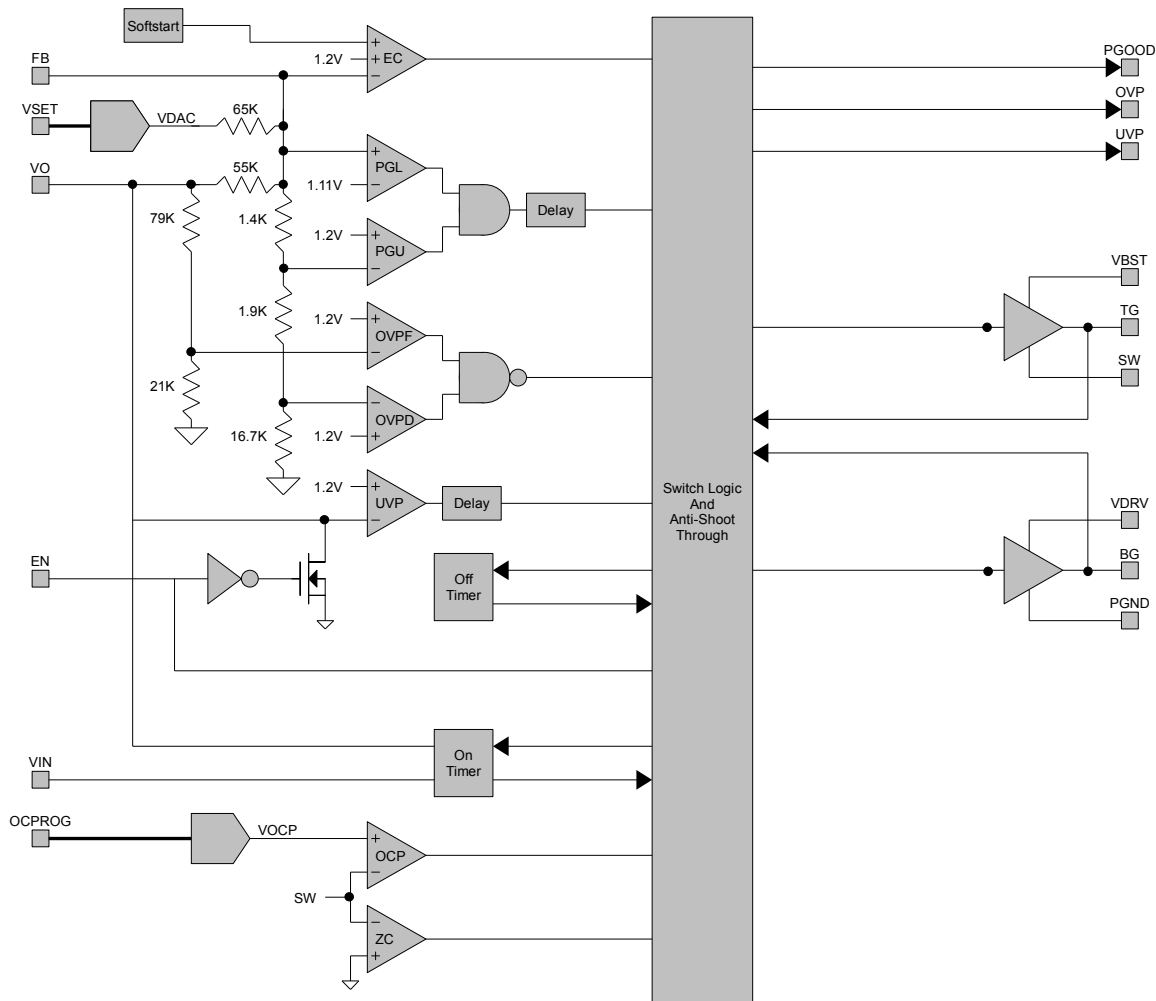
1 Functional Diagram



2 Synchronous PWM controller

This is a high efficiency constant on time input voltage feed-forward step-down synchronous PWM controller. The controller automatically switches between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending on the average inductor current. In CCM, the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. The top external MOSFET remains on for a fixed amount of time that is dependent on the input and output voltage relationship. When the top external MOSFET is turned off, the bottom external MOSFET is turned on until the inductor current is less than the valley current limit and the error comparator shows that output voltage is in error.

In DCM, the inductor current is not allowed to reverse. Therefore, the bottom MOSFET is turned off when the inductor current reaches zero. Both the top and bottom external MOSFETs remain off until the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. During the time that both external MOSFETs are turned off, the output voltage is supplied by the output capacitor.



2.1 On-Time Control

The on-time of the PWM controller is dynamically adjusted on a cycle-by-cycle basis to maintain a constant ripple current in the power inductor. The input and output voltage of the switching regulator is monitored to adapt the period of a one-shot timer that sets the on-time of the controller. The typical on-time is:

$$t_{ON} = \frac{5.83 \mu V_s}{V_{IN} - V_{VO}}$$

2.2 DCM Operation

During light load, the PWM controller enters DCM to maintain high conversion efficiency. DCM is entered when the inductor valley current reaches zero and the bottom external MOSFET is turned off to prevent the inductor current from reversing. This decreases the effective switching frequency of the controller and reduces conversion losses in the MOSFET drivers. When both the top and bottom external MOSFETs are off, the output voltage is maintained by the output capacitance. Once the light

load discharges the output capacitance to the point where the error comparator detects that the output voltage is in error, a new switching cycle is started by tuning on the top external MOSFET. The on-time is not effected. The load current where the controller transitions between CCM and DCM is:

$$I_{OUTx} = \frac{1}{2} \left(\frac{V_{VIN} - V_{VO}}{L} \right) t_{ON}$$

When operating in DCM, the effective switching frequency is dependent on the load current. The approximate switching frequency is:

$$f = \frac{I_{OUT}}{\left(\frac{V_{VIN} - V_{VO}}{2L} \left(t_{ON} + \frac{V_{VIN} - V_{VO}}{V_{VO}} \right) \right)}$$

The maximum time both external MOSFETs can remain off while in DCM mode is limited to 1026μs. In the event of a DCM timeout, the bottom external MOSFET is turned on first for the minimum off-time to recharge the boost capacitor. Subsequently, the top external MOSFET is only turned on if the error comparator detects that the output voltage is in error.

2.3 External Ripple Injection

External ripple injection circuitry may be required to generate sufficient voltage ripple at the VFB pin. This is necessary to minimize jitter in the switching frequency.

2.4 MOSFET Drivers

Both the top and bottom MOSFET drivers are designed to drive N-channel external power MOSFETs. The bottom MOSFET driver pulls BG down to PGND to turn off the external MOSFET, and it pulls BG up to VDRV to turn on the external MOSFET. Likewise, the top external MOSFET driver pulls TG down to SW to turn off the external MOSFET, and it pulls TG up to VBST to turn on the external MOSFET. The combined power dissipation of both MOSFET drivers in a the PWM controller attributed to switching events is:

$$P_{DIS} = V_{VDRV} \times f \times (Q_T + Q_B)$$

where f is the switching frequency, Q_T is the gate charge of the top external MOSFET, and Q_B is the gate charge of the bottom external MOSFET.

The top MOSFET driver has a floating power supply $V_{VBST} - V_{SW}$ that is derived from the 5V supply using a boost capacitor and boost diode. The boost capacitor is recharged through the boost diode from the 5V supply when ever the bottom external MOSFET is turned on and SW is pulled to PGND.

2.5 Anti-Shoot Through Circuitry

In a synchronous pwm topology, it is possible to get shoot-through current from VIN to PGND when both the top and bottom external MOSFETs are fully or partially conducting. To prevent this, a dead time where both MOSFETs are off is internally generated by adding a delay from the turn off of the top external MOSFET to the turn on of the bottom external MOSFET and from the turn off of the bottom external MOSFET to the turn on of the top external MOSFET. The voltage and discharge current of both the top and bottom external MOSFETs are monitored to dynamically optimize the driver dead time and increase conversion efficiency.

2.6 Start-Up

The PWM controller is enabled when both the EN and REGEN pins are driven high. When enabled, there is a brief delay while the internal analog circuitry is powered-on and stabilized. Next, an internal DAC linearly ramps the error comparator reference voltage from 0V to VREF. This forces the regulated output voltage to linearly increase from 0V to the final programmed output voltage in 1.5ms.

2.7 Shutdown

The PWM controller is disabled when either the EN or REGEN pins are driven low. When disabled, the internal analog circuitry of the PWM controller is forced into a low power mode. Also, the regulator output is discharged through the VO pin with a internal limited current sink.

2.8 Output Discharge Circuitry

A 10mA minimum output discharge current sink is connected through VO. The output discharge is active when the REGEN pin is driven low. The output discharge circuitry is not active when EN is driven low.

2.9 Powergood

The PGOOD pin is an open-drain output that indicates if the output voltage of the PWM controller, measured at pin VO, is

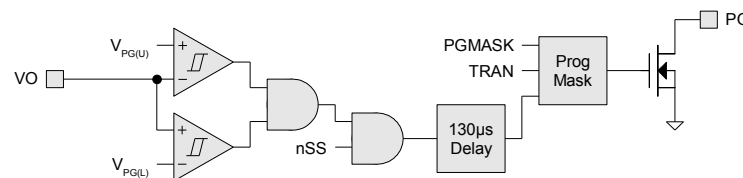
within regulation. In fixed output voltage operation, the PGOOD pin is high impedance if the regulator output is within regulation, and the PG pin is pulled to ground if the regulator output is out of regulation. Additionally, the PG pin is pulled low if the regulator is disabled or operating in soft-start. The power good regulation window is defined in the Electrical Characteristics table.

To minimize the effect of noise on the VO pin, there is an internal fixed 130µs delay on the PGOOD output. Thus, VO must be inside the regulation window for at least 130µs before the PGOOD pin becomes high impedance. However, the PGOOD pin will be pulled low immediately after VO leaves the regulation window.

During controlled output voltage transitions, a programmable masking of the PGOOD signal is enabled. While the On-Demand Power™ controller is ramping either VSET control voltage from one fixed voltage to a new fixed voltage, the PGOOD pin will retain its state previous to the beginning of an output voltage transition until the output voltage is complete. Thus, if the PGOOD pin was pulled low at the beginning of a voltage transition, the PG pin will remain pulled low throughout the entire output voltage transition, even if the transition event causes the output voltage to enter the regulation window. Likewise, if the PG pin was high impedance at the beginning of a voltage transition, the PG pin will remain high impedance throughout the entire output voltage transition, even if the transition event causes the output voltage to leave the regulation window. The programmable mask during output voltage transitions enable the On-Demand Power™ controller to adjust the programmed output voltage VSET at a rate faster than the output of the PWM controllers can respond without inadvertently causing the PGOOD pin to be pulled low.

Furthermore, the programmable mask can be optionally extended for a programmable time period past the completion of an output voltage transition event. This feature allows the PWM controller output voltage some time to settle within the regulation window after a voltage transition occurs. This can be important when the output voltage step is large and/or the slew rate of VSET is high.

The complete powergood logic is shown below. NSS is low when the respective PWM controller is operating in softstart mode. TRAN indicates if VSET for the respective switching regulator is transitioning. PGMASK sets the programmable mask time period.



Powergood logic

2.10 Output Voltage Programming

The regulated output voltage of the PWM controller is controlled with a DAC that is programmed by the On-Demand Power™ controller.

$$V_{VO} = 5 - \left[3 \frac{VSET[7:0]}{256} \right]$$

2.11 Over Current Protection

Over current protection is provided by monitoring the drain-to-source voltage across the bottom external MOSFET when it is turned on. As long as the sensed voltage drop is greater than the programmed voltage threshold, the bottom external MOSFET is forced to remain on. This effectively limits the maximum value of the power inductor valley current.

The over current protection limits is programmed with the OCPROG bits over the SMBus interface. The voltage threshold is temperature compensated to match the temperature dependency of the bottom external MOSFET. The programmed voltage threshold is:

$$V_{TH} = 0.37893(OCPROG + 1)((4.94 \times 10^{-5})T_J + 0.01196)$$

For improved accuracy, there should be a good thermal connection between the MOSFET and the PSG5220.

2.12 Output Over and Under Voltage Protection

The output voltage of the PWM controller is sensed at the VO pin. If the sensed voltage exceeds either the fixed output over

voltage threshold or the dynamic over voltage threshold, the bottom external MOSFET is turned on to discharge the output capacitance and return the output voltage to safe operating level. Once the over voltage condition is no longer sensed, the PWM controller resumes normal operation.

When the sensed output voltage drops below the under voltage threshold, the PWM controller condition is automatically disabled. The EN pin or REGEN pin must be toggled to clear the under voltage condition. This response is desired because an under voltage condition will follow an output short circuit that triggers the over current protection circuitry. This protects the PWM controller and associated circuitry against an output short circuit.

2.13 UVLO Protection

All power supplies are monitored to ensure they are of suitable voltage before the PWM controllers are enabled.

3 Regulator Circuit Design

3.1 Inductor Selection

The maximum load current and inductor ripple current determine the value of the inductor. The value of the inductor ripple current ΔI_L can be calculated with input voltage V_{IN} , output voltage V_O , and on time t_{ON} :

$$\Delta I_L = t_{ON} \left(\frac{V_{IN} - V_{VO}}{L} \right)$$

Since the on-time of the PWM controller is adjusted to maintain a constant ripple current, ΔI_L is determined solely by the inductance value. A lower ripple current improves efficiency by reducing losses in the inductor and ESR losses in the input and output capacitors at the cost of a physically larger inductor. A ΔI_L that is 25% to 50% of $I_{LOAD(MAX)}$ is reasonable for balancing efficiency and inductor size.

An inductor should be selected to have the lowest possible DC resistance to maximize efficiency. Care must be taken to not saturate at the peak inductor current which can be determined by:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

3.2 Output Capacitor Selection

Equivalent series resistance (ESR) is a dominant qualification for output capacitor selection. Specialty polymer capacitors, such as Sanyo POSCAP, are recommended due to high ripple current capability and low ESR at operation frequencies.

Output capacitance should be selected to provide an acceptable output voltage ripple ΔV_{VO} which can be determined by the ESR and magnitude of the output capacitor. The capacitance must be sufficiently large for stability, however the capacitance value relates to the increasing physical size needed to decrease ESR. Consequently, the selection of C_{OUT} is primarily driven by ESR and can be found by:

$$ESR \leq \frac{\Delta V_{VO}}{\Delta I_L}$$

3.3 Input Capacitor Selection

Select the input capacitors based on the expected maximum input ripple RMS current. This current varies with the load and input voltage. The maximum input ripple RMS current occurs at maximum load and can be estimated by:

$$I_{RMS(MAX)} \approx \frac{I_{LOAD(MAX)}}{V_{VIN}} \left[(V_{VO})(V_{VIN} - V_{VO}) \right]^{1/2}$$

3.4 MOSFET Selection

The top and bottom MOSFET should be chosen for low $R_{DS(ON)}$ for increased efficiency, however this must be weighed with increased gate capacitance which increases switching losses. Switching losses are increased in the top MOSFET at high input voltages.

The bottom MOSFET should be placed in parallel with a Schottky diode. Many manufacturers provide a single package device for the MOSFET and diode.

4 On-Demand Power™ Operation

PSG5220 internal registers are programmable via SMBUS to control On-Demand Power™ (ODP) circuitry. Activity on each domain is monitored by current sense and activity inputs. When the ODPEN bit of ODPCON register is set, the output voltage will be managed based on configuration settings, signal on nACT pins, and information gathered from current sensing circuits.

4.1 Output Voltage

Output voltage will vary based on system demand, managed by On-Demand Power™ algorithms.

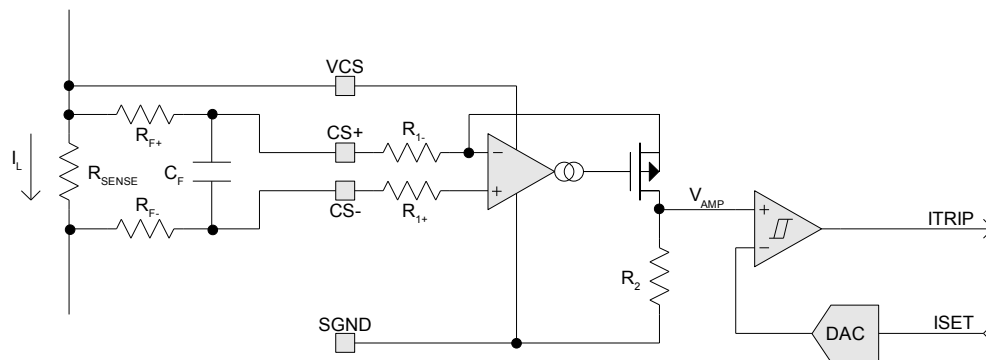
4.2 nACT Inputs

nACT is system control inputs to the On-Demand Power™ algorithm. A low signal on this pin indicates an instantaneous high power mode. The algorithm will interpret this signal to immediately scale to the highest power, highest voltage state.

nACT is design to operate on logic levels from 1.8V to 5V. They should be pulled up to 1.8V when used with SATA hard disk drives. Do not leave nACT. Pull-up to 1.8V when not in use.

4.3 Current Sense

The load current sense circuit detects if the load current I_L is above or below a programmable threshold I_{TRIP} . A high-side current sense amplifier gains the voltage V_{CS} across a sense resistor R_{SENSE} in response to the load current I_L . The output of the current sense amplifier is compared to a programmable threshold voltage V_{TRIP} that is set using an internal 8-bit DAC. The output of the comparator circuit is high if I_L is greater than I_{TRIP} and low if I_L is less than I_{TRIP} . The comparator includes internal hysteresis to help reject noise.



Current sense circuitry (one channel)

The load current sense resistor R_{SENSE} should be selected such that the maximum voltage drop $V_{CS(MAX)}$ across the sense resistor does not exceed the maximum differential input voltage of the current sense amplifier. For a maximum load current of I_{MAX} , the maximum value of R_{SENSE} is:

$$R_{SENSE(MAX)} = \frac{V_{CS(MAX)}}{I_{MAX}}$$

Likewise, the minimum value for R_{SENSE} depends on the minimum load current $I_{TRIP(MIN)}$ that must be detected:

$$R_{SENSE(MIN)} = \frac{V_{CS(MIN)}}{I_{TRIP(MIN)}}$$

The positive and negative sense traces should be routed as a differential pair and Kelvin connected to the sense resistor.

The inclusion of the input low-pass filter helps to smooth spiky load current and reduce the effects of capacitive and inductive noise coupled into the sense traces on the PCB. Adding a capacitor C_F between the CS+ and CS- pins in addition to the input resistors R_{F+} and R_{F-} forms a single pole low-pass differential filter with a cutoff frequency of:

$$f_c = \frac{1}{2\pi(R_{F+} + R_{F-})C_F}$$

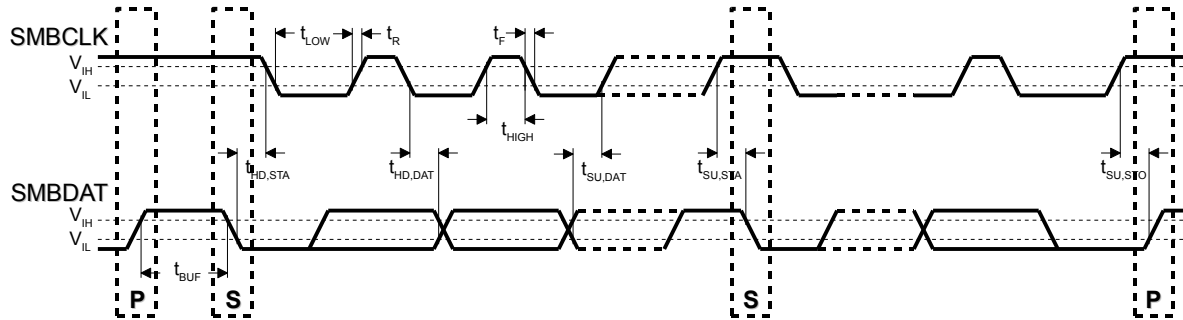
The additional amplifier input offset voltage induced by input resistors R_{F+} and R_{F-} is:

$$V_{OS} = I_{CS-}R_{F-} - I_{CS+}R_{F+}$$

5 SMBus Interface

The PSG5220 serial interface is SMBus 2.0 compliant. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5220 is configured as a slave on the SMBus and has a fixed 7-bit slave address of 0x61. PSG5220 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

5.1 Timing Diagram



5.2 Address Map

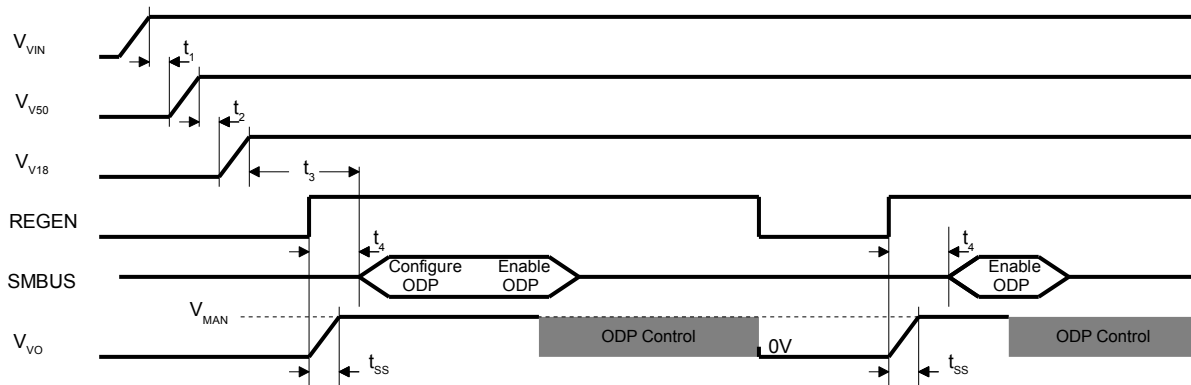
ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
00H	RESERVED								RESERVED	
01H	RESERVED								RESERVED	
02H	RESERVED								RESERVED	
03H	AT_EN	0	0	0	REGEN	ODD	RESERVED	ODPEN	ODPCON	0x08
04H	0	0	0	AT_DN	PGOOD	RESERVED			ODPSTAT	0x00
05H	Regulator Manual Output Voltage								ODPVMAN	0x00
06H	ODP Output Voltage 0								ODPVOUT0	0x00
07H	ODP Output Voltage 1								ODPVOUT1	0x00
08H	ODP Output Voltage 2								ODPVOUT2	0x00
09H	ODP Output Voltage 3								ODPVOUT3	0x00
0AH	Regulator Manual Current Threshold								ODPIMAN	0x00
0BH	ODP Current Threshold 0								ODPITH0	0x00
0CH	ODP Current Threshold 1								ODPITH1	0x00
0DH	ODP Current Threshold 2								ODPITH2	0x00
0EH	ODP Current Threshold3								ODPITH3	0x00
0FH	ODP Step value for incrementing slew rate of output voltage								ODPSTEPUP	0x00
10H	ODP Step value for decrementing slew rate of output voltage								ODPSTEPDWN	0x00
11H	ODP power good blank time								ODPPGBLANK	0x00
12H	ODP Timeout 0 [7:0]								ODPTOUT0_0	0x00
13H	ODP Timeout 0 [15:8]								ODPTOUT0_1	0x00
14H	ODP Timeout 0 [23:16]								ODPTOUT0_2	0x00
15H	ODP Timeout 0 [31:24]								ODPTOUT0_3	0x00
16H	ODP Timeout 1 [7:0]								ODPTOUT1_0	0x00
17H	ODP Timeout 1[15:8]								ODPTOUT1_1	0x00
18H	ODP Timeout 1 [23:16]								ODPTOUT1_2	0x00
19H	ODP Timeout 1 [31:24]								ODPTOUT1_3	0x00
1AH	ODP Timeout 2 [7:0]								ODPTOUT2_0	0x00
1BH	ODP Timeout 2[15:8]								ODPTOUT2_1	0x00
1CH	ODP Timeout 2 [23:16]								ODPTOUT2_2	0x00
1DH	ODP Timeout 2 [31:24]								ODPTOUT2_3	0x00
1EH	ODP Auto threshold count value								ODP1AT_CNT	0X00
1FH	ODP SLEW_CODE[3:0]				ODPTMR_CODE				ODPTMRNSLEW	0X00
20H-40H	RESERVED								RESERVED	

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
41H	0	0	SS[1:0]		OCPROG[3:0]				VREG_CON	0x00
42H	RESERVED								RESERVED	
43H	0	0	0	0	ANA EN_STA T	PG STAT	OVP STAT	UVP STAT	VREGSTAT	0x00
44H-FFH	RESERVED								RESERVED	

6 Operating Sequence

A typical control sequence for the PSG5220 is:

- Apply V_{VIN} and V_{V50} Note: V_{VIN} needs to be powered before V_{V50}
- V_{V18} is supplied from the internal 1.8V LDO
- Enable PSG5220
- Configure ODP control of PSG5220 through SMBUS
- Optionally configure V_{MAN} to another voltage by writing to ODPxVMAN. Output voltage will change immediately.
- Enable ODP by writing 1 to ODPEN of ODPxCON. Output voltage will be under ODP control immediately.
- SMBUS will not operate before t_3 and t_4 have expired.



Start-up sequence minimum timings:

- $t_1 = 0s$
- $t_2 = 0s$
- $t_3 = 250\mu s$
- $t_4 = 250\mu s$
- $t_{ss} = 1.5ms$

Power Down Sequence: Remove V_{V50} before V_{VIN} .

7 Typical Applications

7.1 Application – Intel Mobile Platform

The PSG5210 is well suited for use into the Intel mobile platform. Appropriate connections must be made by the system designer for connection to the mainboard power delivery system, bus architecture, and to hard-disk drives (HDD) and optical-disk drives (ODD). For optimal performance, the current sense resistor and current sense circuitry should be sized appropriately for the type of drive that will be powered by the channel. For example, a smaller sense resistor should be used for a higher power drive to ensure the input differential voltage of the current sense circuit remains in the working range.

Connections to Power

Description	Voltage	PSG5220 Lead	Intel Mobile Platform
Analog Input Supply Voltage	5V	V50	V5.0A
Input Voltage	7.5V to 24V	VIN	Battery/Brick
I/O Voltage	5V	VDDIO	V5.0A
Digital Input Supply Voltage	1.8V	V18	N/A

The switching regulator input voltage is supplied from the battery/brick input voltage to the mobile platform. Since the PSG5210 supports a very wide input range, the system is not required to support narrow voltage direct current (NVDC).

Analog circuitry in the PSG5210 operates at 5V. It is required that this be supplied externally and remain 'ON' in all operational and sleep states. Connect this to V5.0A.

The I/O for the PSG5210 are designed to operate at 5V. Connect these to V5.0A.

Internal digital logic is powered at 1.8V. The PSG5210 supplies this voltage through an internal LDO and should not be connected to an external 1.8V supply. The LDO output, LDO1V8, must be connected to VDD and be appropriately decoupled as described in this document.

Connections to I/O

The PSG5210 manages the voltage supplied to the drive based on information gathered from sensing current and activity feedback on the bus. nACT provides activity information from HDD devices to PowerSage™. HDD devices should support the optional activity indication on pin P11 of the SATA power connector. Connect the activity indicator signal to nACT with a 10k pull-up resistor to 1.8V at LDO1V8. The PSG5210 will operate without the nACT signal on HDD devices but will provide less energy savings. Do not leave nACT floating. Pull-up to LDO1V8 when not in use. nACT is left unconnected for ODD devices.

Communication to the register map is provided through the SMBus interface through pins SMBDAT and SMBCLK. System designers can choose to connect this directly to the Platform Controller Hub (PCH) or through an SMBus hub. The SMBus pull-up resistors should be connected to 3.3V through V3.3A or V3.3S.

Configuration Registers

A number of configuration registers must be set for the PowerSage™ logic to run properly in PSG5210. Voltage, threshold, and timeout registers can be set through the SMBus interface. Packet Digital can supply the appropriate configurations for specific HDD and ODD devices. Additionally, an automatic configuration program is scheduled to be available on future releases.