DUAL SECURE DESIGN FOR POWER FAILURE PROTECTION (PFP)

Silicon Power implemented dual secure design for power failure protection

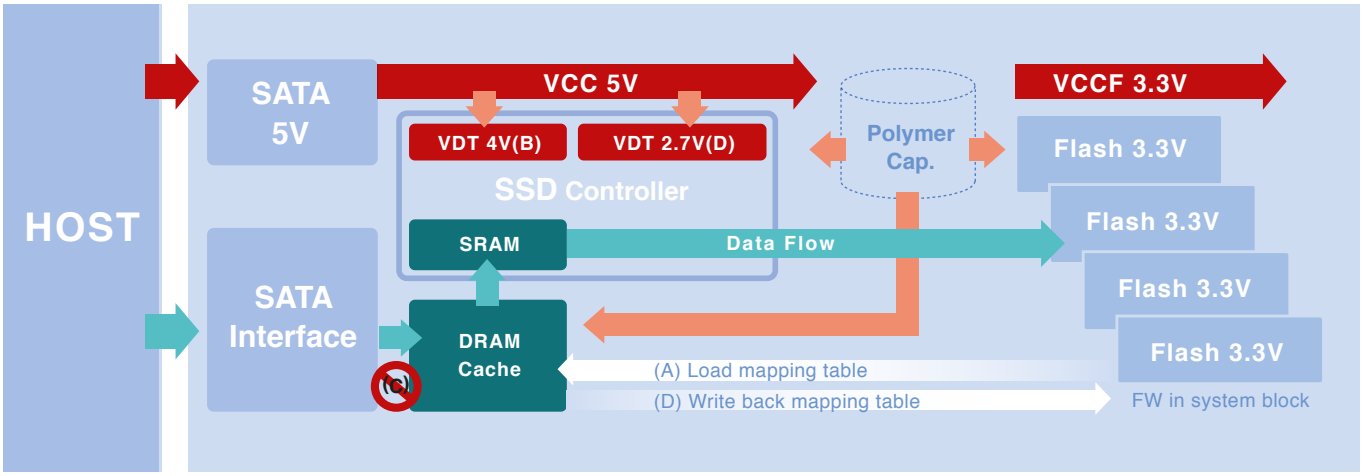
- All series of SP Industrial SSD with Power shielding firmware architecture protection when sensing unstable voltage and power down to stop receiving host commands.
- R series of SP Industrial SSD implements Advanced PFP with industrial grade polymer capacitors to gain more time for the data flushing process from DRAM cache to Flash, under sudden power off situations.

How SSD controller manage power failure?

SSD FW stored inside NAND Flash called system block. When System power on, SSD will load related mapping table and initial commands into DRAM for SSD controller (Figure 1-A). When VCC is under 4V (Figure 1-B), SSD Controller will enable the power shielding function, during this period the SSD controller will start to flush DRAM cache data save into FLASH to secures the user data in a limit time. At the same time VCC <4V SSD controller will stop receiving command from Host (Figure 1-C) to protect itself. Host can not recognize SSD and SSD stop working during this period until VCC resumes and become stable.

When VCCF is under 2.7V (Figure 1-D), SSD controller will initial flush command to write back mapping table back to flash system block. During this period Host can not recognize SSD. SSD still can not work even power resumes. Need to turn Power ON/OFF again for host to restart SSD work normally. During SSD operation, data is temporarily stored in the DRAM cache to reduce the performance gap between the host interface and the NAND Flash memory. However, in cases of unexpected sudden power loss, such as unplugging the power to the system, sudden battery loss or unplugging devices from the system, the flushing process cannot be completed and may cause serious device failure. Silicon Power Dual secure design for power failure protection (PFP) resolves such issue with firmware-based protect mechanism and capacitor backup circuit.

Figure 1 Different techniques for erasing data from SSDs



Design concept of Advanced PFP

In case of SP 2.5” Industrial SSD R Series 512GB under continuous writing mode. When VCCF drops from 5V to 4V, Power Shielding function will be enabled and SSD controller will stop receiving the SATA Host command. If VCC is not able to be substantiated and continue dropping to 2.7V, SSD needs 10ms estimated time to complete following program processes to secure SSD’s integrity.

- 3ms: Controller flushes user temp data in DRAM buffer area (2MB) and program into NAND Flash.
- 2ms: Controller flushes QBT table in DRAM cache and program into NAND Flash.
- 5ms: Controller flushes Linking tables in DRAM cache and program into NAND Flash (only for SKUs with DRAM).

SP implemented Advanced PFP with 6 pieces of Polymer Tantalum Capacitor 470uF as a backup battery to sustain 4V@250mA for about 10ms to complete the above program processes

According to the following calculation the Advanced PFP capacitor can maintain 4V@250mA for about 10ms when VCC drops from 4V to 3.3V. (Figure 2)

Figure 3 shows the Power Timing Chart of SP 2.5” Industrial SSD R Series 512GB under continuous writing mode. Advanced PFP circuit has capability of hold time as followings:

- 10.1ms hold time when VCC drops from 4V to 3.3V
- 20.5ms hold time when VCC drops from 4V to 2.7V

Figure 2

Circuit simulation of Advanced PFP design

Cap height limination	H≦	4.3	mm
Total hold up time	T=	10	ms
Charge voltage	V1=	4.0	Volt
Stop voltage	V2=	3	Volt
Output Power	P=	1.00	Watt
Minimum	Vr=	2.7	Volt
Total Energy	E=	10.0	mJ
Total Capacitance	C=	2,857.1	uF

$$E = P \times T = \frac{1}{2} C\left(V_1{}^2 - V_2{}^2\right)$$

$$C = \frac{2E}{\left(V_1{}^2 - V_2{}^2\right)}$$

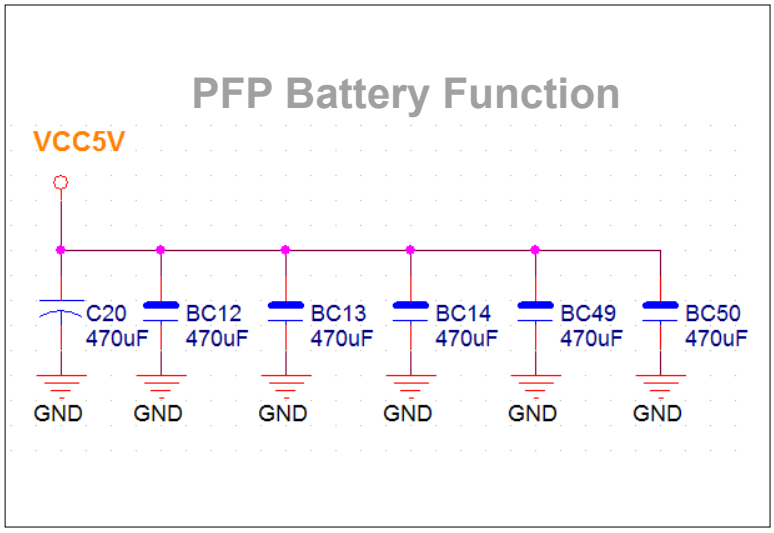
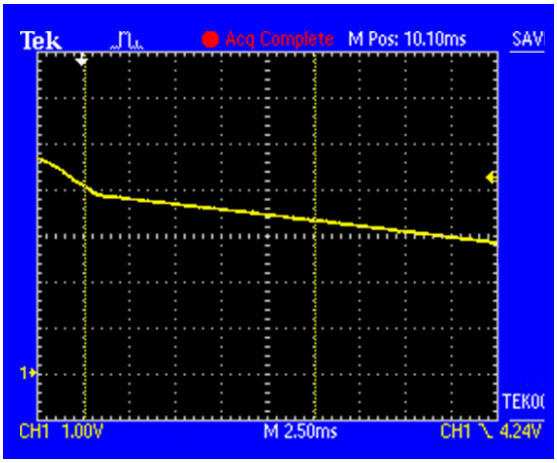


Figure 3

Power Timing Chart of Advanced PFP design under continues sequence writing



How does the Advanced Power Failure Protection (PFP) mechanism work?

Power Shielding function integrates built-in VDT and firmware mechanism. The trigger alert is able to monitor an abnormal power drop and take instant action, such as prohibit receiving data from the Host and backup mapping/linking table into FLASH, as soon as potential power failure is detected.

Advanced PFP is a way to gain more time for the data flushing process from DRAM cache to FLASH under sudden power-off situations by using dedicated polymer capacitor components. These capacitors are charged during power on and offer charged power to the SSD circuit under sudden power-off situations. (Figure 4 & Figure 5)

SP's Advanced PFP technology SSD provides at least 20ms to ensure the data flushing task can be completed within the discharge time. Furthermore, it always passes the Power Cycling test under abnormal conditions at least 3,000 times.

Figure 4

Power Timing Chart of Advanced PFP

Figure 5

Mechanism of Advanced PFP