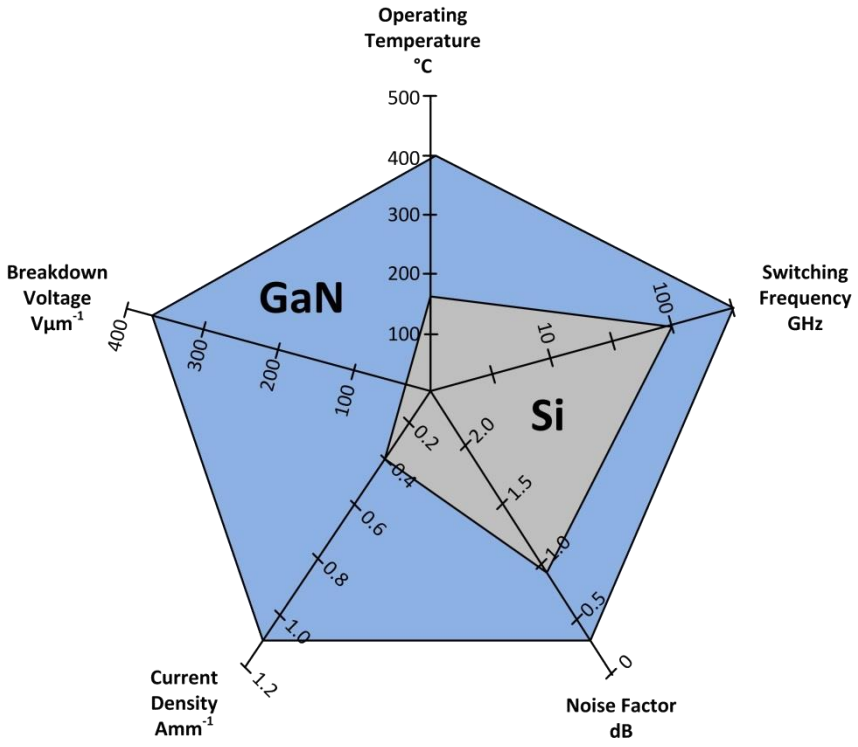
Whitepaper

DC/DC Converters for GaN Gate Drivers



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Gallium Nitride (GaN) semiconductors are High Electron Mobility Transistor (HEMT) devices, a class of transistors with almost perfect switching characteristics. HEMT means that electrons travel within the internal crystal structure as a two dimensional electron gas with very high mobility, thus creating a device with very high conductivity and low RSDON. The use of GaN chemistry increases the breakdown voltage which means that the layers within the transistor can be made very thin and close together. This both accelerates the switching speed and reduces the gate capacitance.

The enhancement mode type (E-HEMT) has a depletion zone under the gate which blocks the flow of electrons and requires a positive gate voltage with respect to the source pin to turn on. As the depletion zone under the gate is so thin, very little injected charge is needed to turn the transistor on and off, so switching speeds in the MHz region are possible without incurring high switching losses.

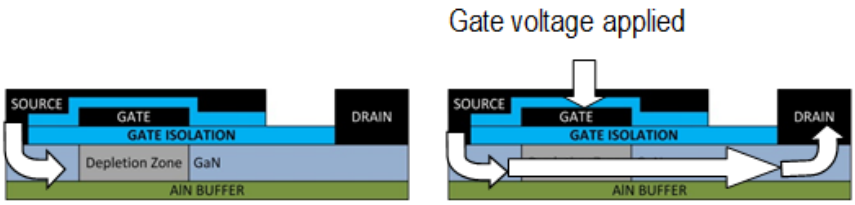

Figure 1: Diagrammatic layout of an Enhancement Mode GaN Transistor in the OFF and ON conditions

The extreme thinness of the gate isolation layer means that high gate-source voltages will cause an internal flashover, even though the material itself has a high breakdown voltage rating. A GaN E-HEMT has a typical full enhancement voltage of 7V but will be damaged if the VGS exceeds ±10V, much lower than the gate voltages that are typically used in IGBT or SiC gate drivers. Due to the extremely fast rise and fall times of the low-capacitance gate channel, any excessive inductance in the external gate drive could cause spikes or voltage ringing and exceed these voltage limits. Therefore a 6V gate drive voltage is a good compromise between high efficiency and staying within a safe operating area.

IGBT or SiC gate drive circuits also typically turn off with a negative gate drive voltage. This speeds up the charge extraction from the gate capacitance and therefore the switch-off time. GaN Transistors have such low gate capacitance that a negative gate drive is not necessary. A gate voltage of 0V will completely and reliably turn off the HEMT in nanoseconds. Only if the layout has excessive inductance would a negative gate drive offer protection against unintentional turn-on caused by ringing. However, as HEMT do not have a body diode like a MOSFETs and are symmetrically conductive devices, a negative gate voltage will increase reverse conduction losses. A single ended 6V-0V gate drive voltage is ideal.

Figure 2 shows typical gate driver voltages that are commonly used. The 1st Generation SiC MOSFETS use +20/-5V supplies, but 2nd Generation devices will most likely use +15/-3V supply voltages:

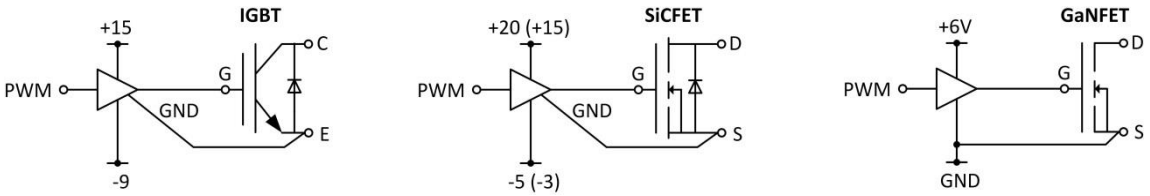

Figure 2: Typical Gate Driver supply voltages for IGBT, SiC and GaN drivers

2 GaN Gate Drive Considerations – Design Guidelines

1: The majority of ultrafast gate drivers ICs have an under-voltage lock-out (UVLO) function that disables the output if the supply voltage is too low. Those meant for IGBT/SiC applications will often have a relatively high UVLO level as they are designed to operate from supply voltages up to 24V. A gate driver that is compatible with the much lower gate voltages used in GaN must be selected.

2: The current needed to charge and discharge the gate capacitance is dependent on the gate capacitance and the rate of change of the gate voltage. Although the GaN gate capacitance is very low, the high dv/dt means that a gate driver with a current drive capability of at least ±0.5A (or better 1A sink) is required. This peak current will be supplied from a ceramic capacitor mounted as close to the driver pins as possible, so the average supply current will be much lower (in the tens of milliamps range). The gate driver sink drive should be low-impedance (<2 Ohms) to reduce the chance of cross-conduction (see next comment).

3: An ultrafast gate drive design is susceptible to undesired turn-on (cross-conduction) due to parasitic gate driver inductances interacting with the high Miller capacitance discharge current thus creating a ringing oscillation that could send the gate voltage momentarily high again. The slew rates can be limited by a dv/dt limiting resistor to reduce the possibility of this effect. A turn-on gate resistor in the range of 10-20 Ohms will typically give a 80-40kV/µs slew rate. The turn-off resistance should be smaller to reduce the turn-off losses. A Schottky diode with a resistor in parallel with the gate resistor can be used to independently control the turn-on and turn-off slew rates (Figure 3).

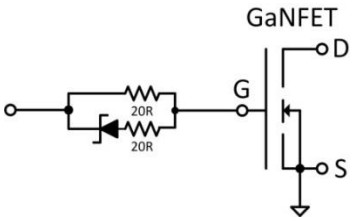

Figure 3: Slope control using gate resistors

4: High side gate drivers are often implemented with a bootstrap power supply circuit (figure 4). Although this means that the same isolated power supply can be used for both high-side and low-side drivers, it has some inherent weaknesses.

The bootstrap diode must have an ultrafast recovery characteristic. If it cannot switch off as quickly as the GaN output then a reverse current will flow back into the VDD supply. Not only will these current spikes affect the lifetime of the diode, but the resulting high frequency interference on the supply rail will cause havoc with the EMC compliance.

The gate driver bootstrap supply voltage is dependent on the difference between the VDD supply and the capacitively-coupled output (switching node) voltage. This means that the voltage across the bootstrap capacitor can vary by more than ±20% during operation.

There will be a volt drop across the high voltage bootstrap diode of around 0.8-1.0V meaning a 7V supply is needed to give the required VDDH voltage of 6V. However, the switching node voltage can go as high as +0.5V during forward conduction, meaning that the effective gate driver supply voltage is only 5.5V. If the gate driver supply voltage is too low, the GaN HEMT will not be fully enhanced and the conduction losses will be higher. This condition is especially critical in burst mode or for the initial pulse after turn-on when the bootstrap capacitor may not be fully charged due to the narrow first pulse.

However it is not advisable to increase the supply voltage to 7.5V to guarantee a minimum 6V VDDH voltage because during reverse conduction conditions, the switching node voltage can bounce to as much as -2.5V below ground, meaning the effective bootstrap voltage becomes +6.5V +2.5V = 9V. This is getting perilously close to the absolute maximum gate voltage of 10V. The interaction with the load current and parasitic inductances can additionally cause negative-going spikes to be generated at the switching node by high di/dt transitions, creating operating conditions where the bootstrap voltage will exceed 10V when these transients are also taken into account.

Bootstrap voltage varies between 5.5V and 9V depending on choice of VDD and

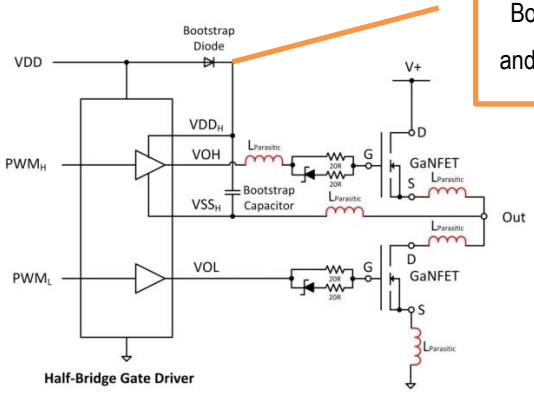

Figure 4: Typical high-side bootstrap supply circuit showing unwanted parasitic inductances

A more reliable solution is to use a separate galvanically isolated supply for the high-side gate driver. This will ensure a stable gate voltage irrespective of the operating conditions.

5: Gate driver inductances can be minimized by good design, but it is more difficult to control the parasitic inductances of the power ground as the layout choices for high current paths are more restricted. Although a low-side switching circuit has common power ground and gate driver ground, any parasitic layout inductances will create ground bounce under high di/dt conditions. For operational safety, it is therefore advisable also to galvanically isolate the low-side drivers as well as the high-hide drivers. If the gate drivers are isolated, then the influence of the layout power ground inductances can be eliminated by connecting the gate driver ground directly to the transistor source connection (or to the Kelvin connection if this is supported in the transistor package).

6. The PWM isolator and galvanically isolated DC/DC converter should have low isolation capacitance. The high dv/dt slew rates and switching frequencies possible with GaN devices will stress the isolation barrier, even if the absolute voltage swings are well within the voltage ratings of the components. For high dv/dt applications, the isolation capacitance should be <4pF for the PWM isolator and <10pF for the high side DC/DC converter. If a DC/DC converter is also used on the low side to eliminate ground bounce, then the isolation capacitance is not so critical, however an isolation capacitance of <100pF is desirable.

3 Example Gate Driver Circuits

Notice: RECOM cannot assume responsibility for the following circuit examples, which may be incomplete. However, they are presented in good faith based on our knowledge of high speed driver design. The PCB layout is absolutely critical. The effects of stray capacitances and parasitic inductances can affect the performance of the design significantly. As with all high voltage designs, take great care to incorporate sufficient safety measures and adequate fault protection.

3.1 Application Example: Isolated Power Switch

This fully-isolated design uses a DC/DC converter and digital isolator to create a gate driver circuit for a GaN HEMT that could be used as a boost converter, buck converter or buck/boost converter switching element. The single-channel digital isolator output stage is powered from a low power LDO regulator connected to the 6V gate driver supply. The UCC27322 high speed driver can deliver up to ±9A peak current and the Schmitt-trigger input switches cleanly from the 5V output of the digital isolator. A dead-time delay can be implemented with a simple RC filter. Supply overvoltage protection (OVP) is provided by a Zener clamp.

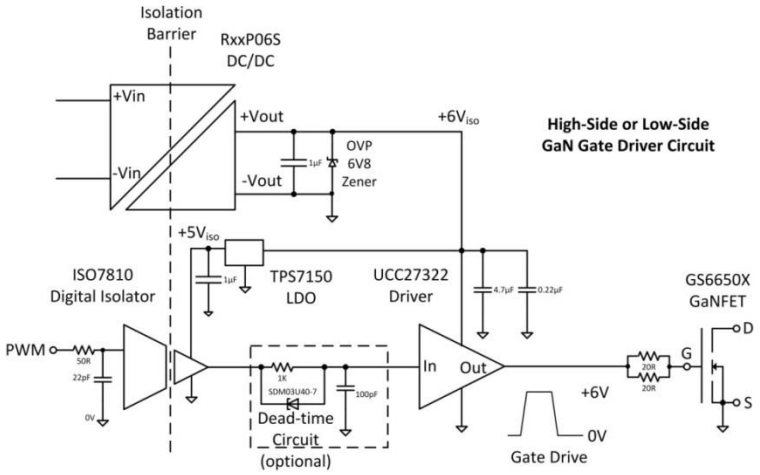

Figure 5: Example of a GaN isolated power switch

3.2 Application Example: Half-Bridge Power Stage

This fully-isolated design uses two DC/DC converters and dual channel digital isolator to create a half-bridge gate driver circuit for a GaN HEMT that could be used in an inverter, power converter or motor controller application. The dual-channel digital isolator contains a built-in overlap protection circuit with a resistor-programmable dead-time control. The high side and low side drivers are independently isolated from both the input and each other, eliminating feed-through from one power stage to the other.

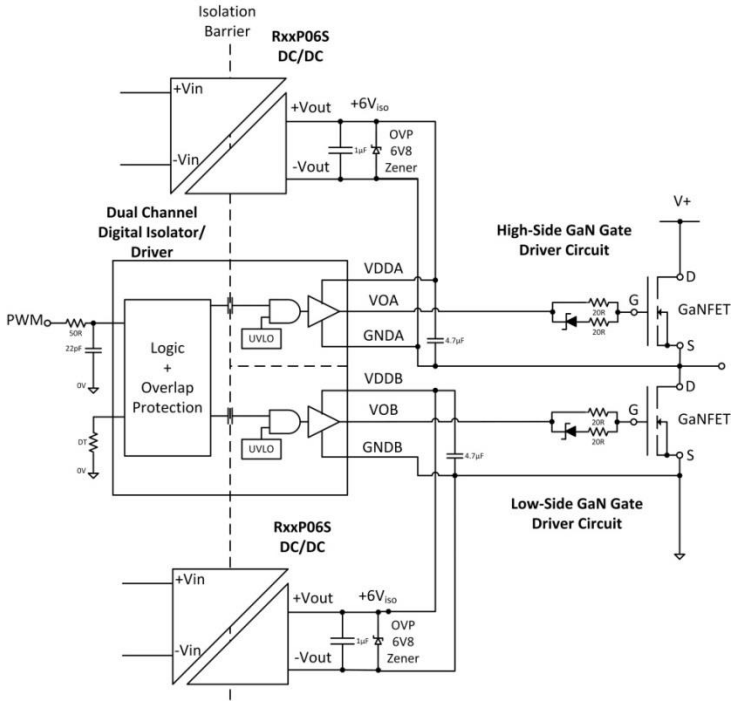

Figure 6: Example of a fully isolated GaN half-bridge power stage

3.3 Application Example: Bridgeless PFC

This bridgeless totem pole PFC circuit uses two half bridge power stages to replace the bridge rectifier and the PFC switcher normally required by AC powered applications. The synchronous rectifier consists of two silicon MOSFETs alternately switched with a 50% duty cycle at 50/60Hz in time with the AC mains input. This creates a rectified output without the need for an input bridge rectifier. The PFC half-bridge circuit runs with a higher frequency and variable duty cycle PWM signal to perform the power factor correction function using low loss GaN transistors. Such designs can deliver up to 99% efficiency as there are no power diode losses.

With the low component count, the gate driver components can be placed closer together and parasitic inductances and stray capacitances can be minimized. Two RP-1506S converters and a dual channel digital isolator are used to create the fully isolated high speed half-bridge GaN gate driver circuit for the high frequency PFC circuit. The AC synchronous rectification half-bridge runs at the lower frequency of 50Hz or 60Hz, so low cost MOSFETs can be used without sacrificing overall efficiency or performance. All of the isolated gate drivers are powered by RP-15xxS DC/DC converters. The RP series offers high 5.2kVDC isolation and low <10pF isolation capacitance, so are ideal for such applications. The low-side MOSFET gate driver can be supplied directly from the 15V on-board power supply to save cost, as no isolation is needed.

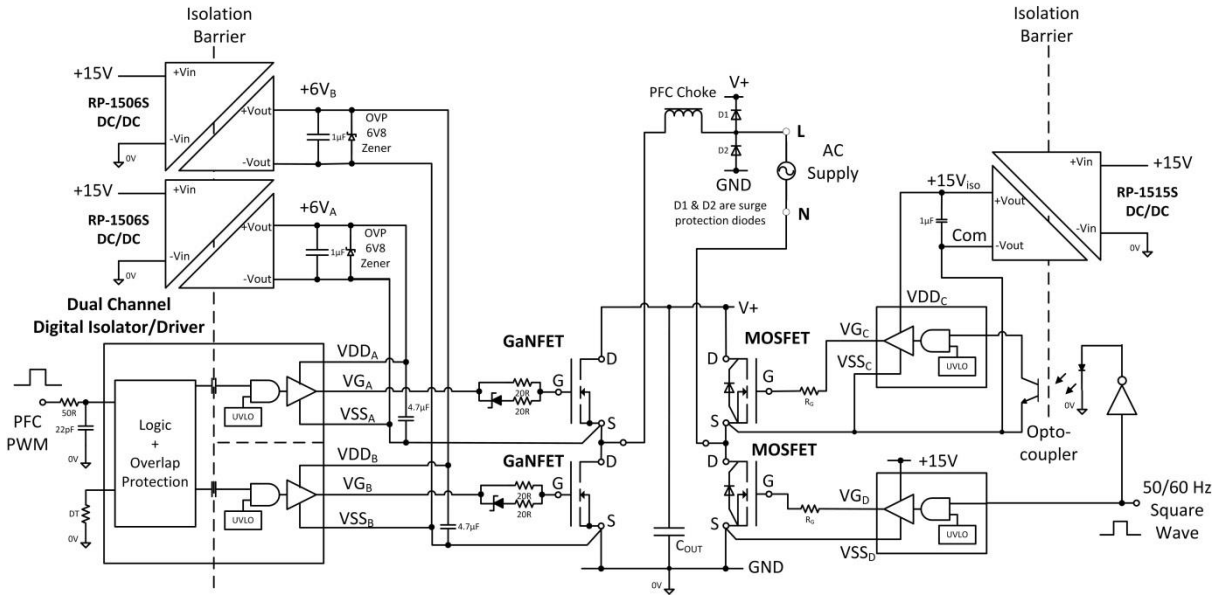

Figure 7: Example of a bridgeless combination GaN/MOSFET PFC rectifier Stage

4 Conclusion

GaN HEMT technology opens up new possibilities for power electronics, promising near perfect switching behaviour with higher efficiency and higher switching speeds. However, with all high frequency designs, the PCB layout and the management of the parasitics are crucial to good performance. The use of low leakage capacitance DC/DC converters to provide the isolated power supply to the gate driver circuits simplifies the design and can eliminate some of the causes of failure in high dv/dt and di/dt GaN applications.