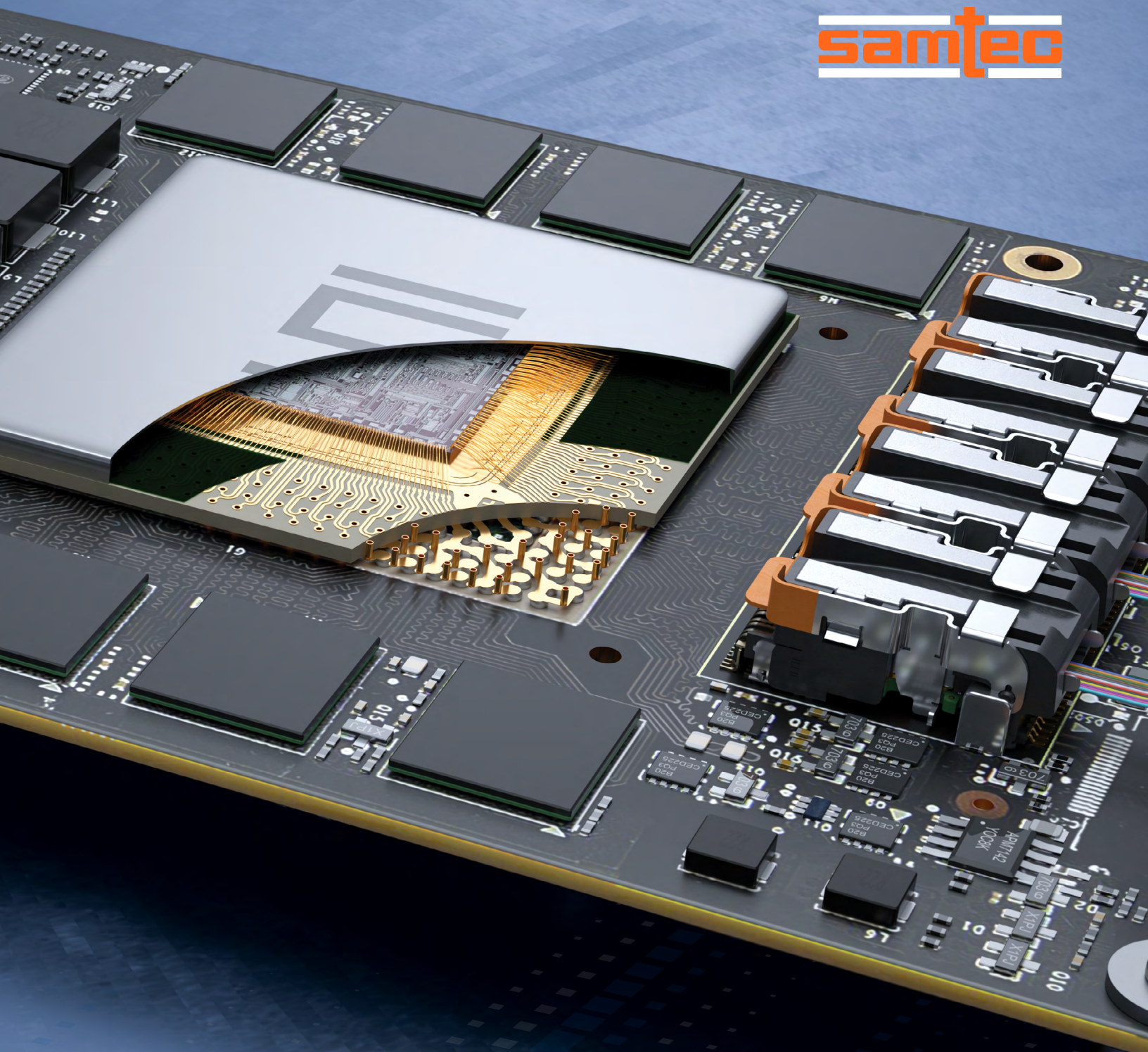




MICROELECTRONICS INTERCONNECT SOLUTIONS GUIDE

MICROELECTRONICS INTERCONNECT SOLUTIONS

Next generation microelectronics require increased performance and integration, advanced chip technology and miniaturization. Samtec's extensive microelectronics and high-speed interconnect expertise, along with our proven methods for package integration, miniaturization, wafer level processing and signal integrity optimization, enable us to provide a unique level of support for advanced microelectronics applications.

MINIATURIZATION

INTEGRATION

SIGNAL INTEGRITY

POWER INTEGRITY

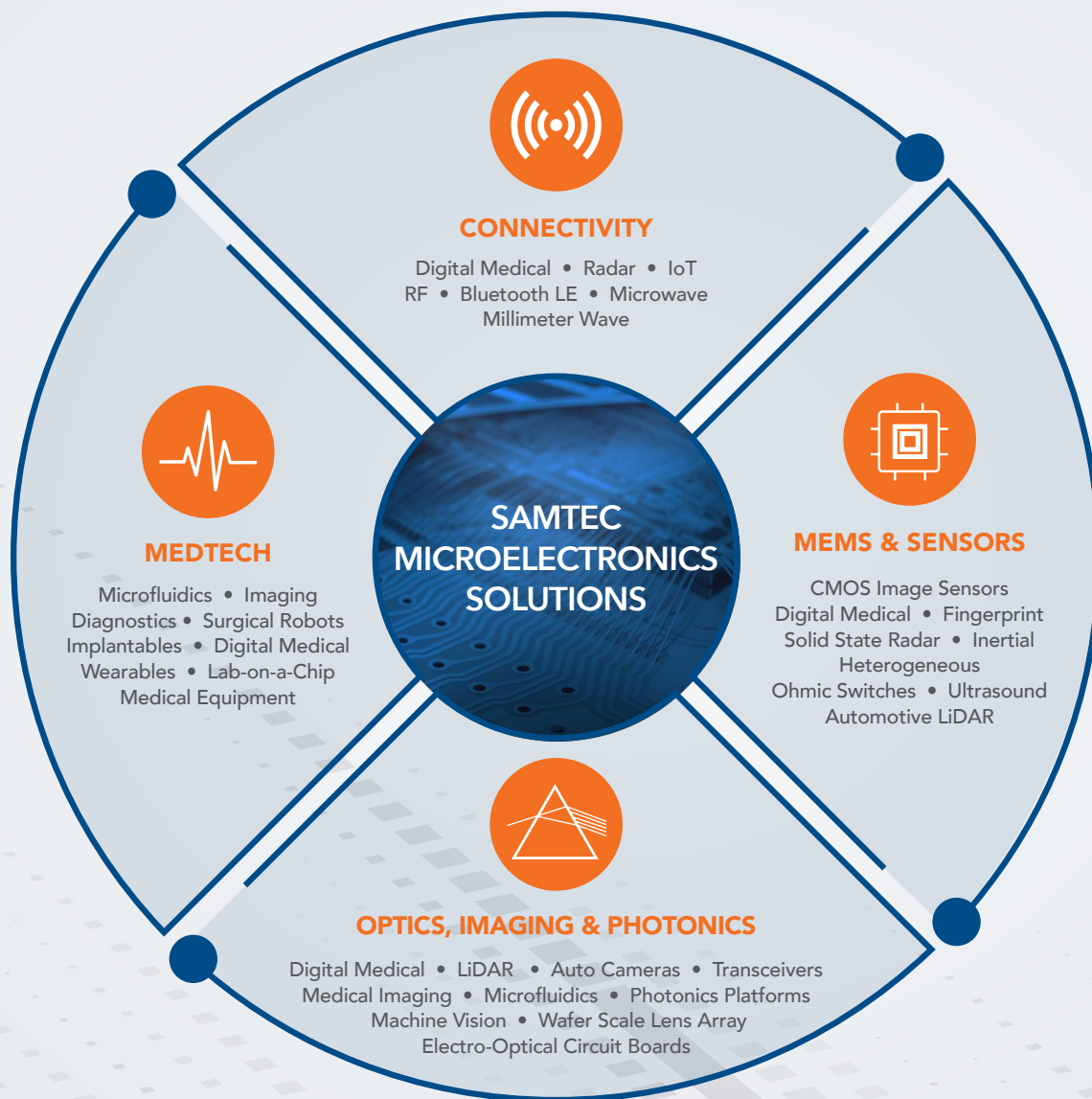
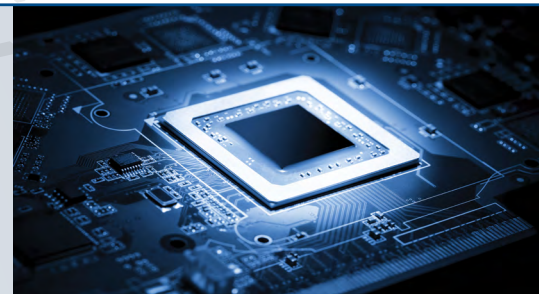


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Redistribution Layer (RDL) Circuit Formation
High Performance Glass-Based Electronics
Glass Core Technology Design Guidelines



MICROELECTRONICS SYSTEM SUPPORT.. 12-13

Support for Full Channel Challenges
Package & PCB Design
Modeling & Simulation
Analysis, Testing & Validation



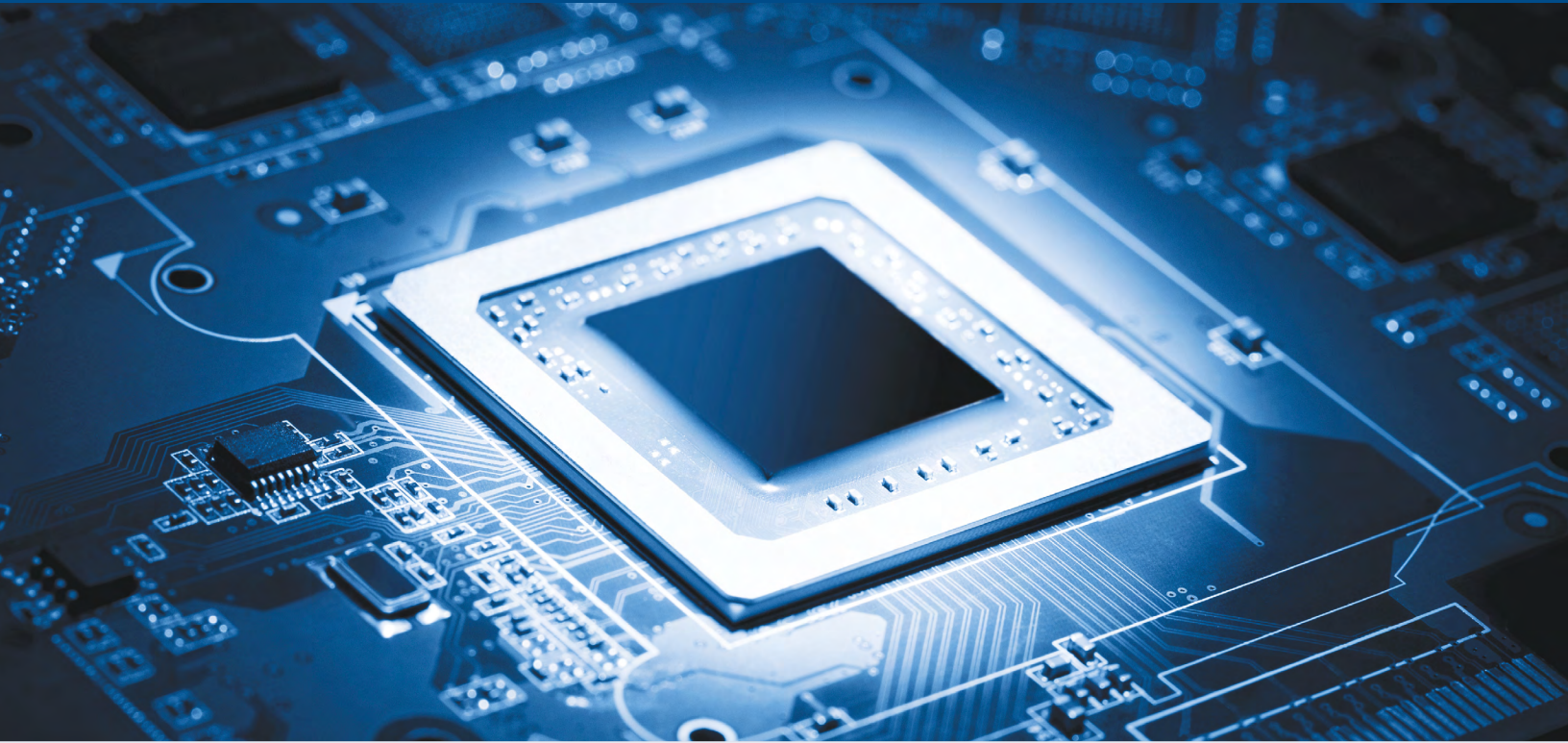
TECHNOLOGY CENTERS..... 14-15

Samtec Microelectronics Group	Samtec Optical Group
Samtec Teraspeed Consulting	Advanced Interconnect Design
Signal Integrity Group	High-Speed Cable Plant



ADVANCED PACKAGE DESIGN

COMPLETE DESIGN & SUPPORT FOR ADVANCED PACKAGING APPLICATIONS



Development

Complete support is available from the early stages of the design process, including:

- Advanced IC Package Design
- Material Selection & Procurement
- Assembly Processing / Compatibility
- Package Reliability / Testing

Prototyping

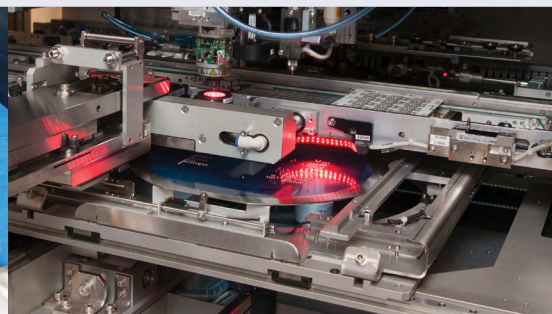
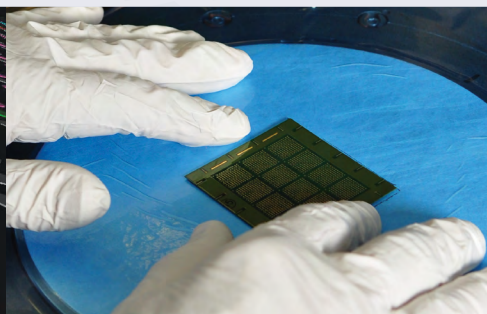
To help get your design to market faster, we offer quick-turn prototyping, along with:

- Initial Concept Builds
- Reasonable NREs
- Industry-Leading Lead-Times
- Minimized Iterations Save Time-to-Market

Production

Full production capabilities support a variety of order volumes and cost-levels:

- High Yield Automation / Production
- Repeatability / Process Control
- Transfer Molding Capabilities
- Asian Subcontractors Provide Flexibility



CORE PACKAGING CAPABILITIES

PRECISION DIE PLACEMENT

High-speed, high accuracy die placement (to +/- 3 microns)

WIRE BONDING

Ultra-fine pitch, ultra-low profile ball bond, wedge bond or ribbon bond

FINE PITCH FLIP CHIP & JET UNDERFILL

Ultra-high bump count; tight keep-out regions between die

ENCAPSULATION

Encapsulating with dam and fill, glob top or transfer molding

ADVANCED PACKAGING & ASSEMBLY

Advanced substrates, inspection & metrology

Glass substrate manufacturing, fan out technology

2.5D / 3D TxV technology

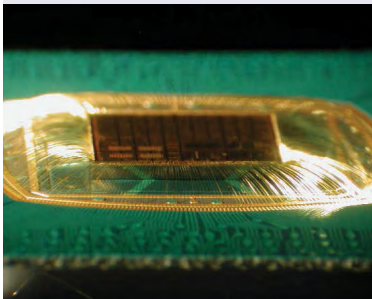
Wafer Dicing - 2" to 8" capabilities; thicknesses down to 25 μm

Solder Ball Attach for tight pitches down to 0.4 mm

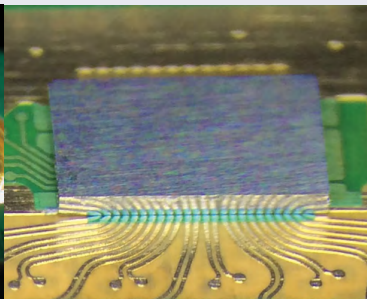
Lid Attach - AuSn solder, glass frit, hermetic, fluidic, optical, custom materials

SEE PAGES 6-7 FOR TYPICAL DESIGN GUIDELINES.

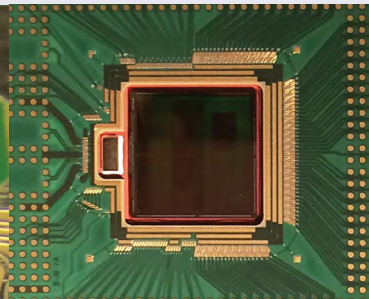
COMPLEX WIRE BOND



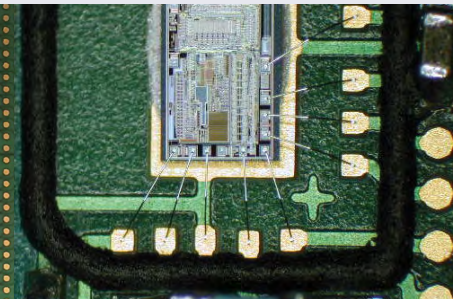
FLIP CHIP & UNDERFILL



PRECISION DIE ATTACH



FINISHING CAPABILITIES

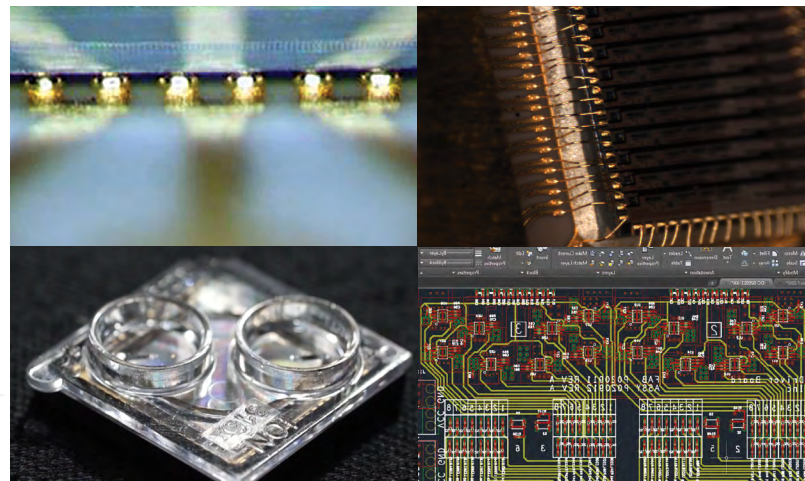


KEY ENABLING TECHNOLOGIES | ROADMAP

Samtec is invested in the development of innovative products and technologies to meet the density and performance demands of next generation microelectronics. Some of our current technologies in development include:

- Thermocompression Bonding
- Gold Stud Bumping
- Anodic Bonding (Wafer-to-Wafer)
- Transfer Molding (conventional and optically clear mold compounds)
- Silicon Photonics and Optics with Ultra-Tight Tolerances

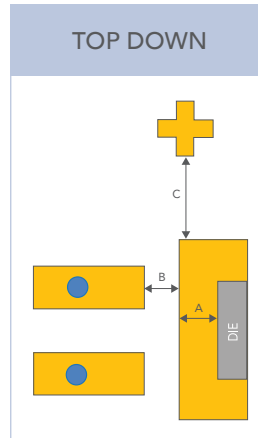
Contact the specialists at Samtec Microelectronics to discuss solutions for your IC Packaging application.



IC PACKAGING & ASSEMBLY DESIGN GUIDELINES

PRECISION DIE ATTACH

- Minimum distance between surrounding square of fiducial and neighboring objects must be 0.048 mm
- Gray level contrast between background and fiducial must be a minimum of 100 gray levels out of 256
- Background of fiducial must not have a structure and background must be single-colored gray level
- Max. die size for dipping: 50 mm x 50 mm
- No waffle-pack handling for die < 1 mm²
- Maximum length to width ratio for components: 5:1



DIE ATTACH REQUIREMENTS (TYPICAL)

	DESCRIPTION	ORGANIC (min)	CERAMIC (min)
	Minimum Die Size	0.010" (250 µm)	0.010" (250 µm)
A	Overlap of Die Attach Ground Plane to Die Edge	0.020" (500 µm)	0.020" (500 µm)
B	Space Between Die Attach Ground Plane to Wirebond Pad	0.020" (500 µm)	0.020" (500 µm)
C	Space Between Fiducial Edge to Die Attach Ground Plane Edge	0.010" (250 µm)	0.006" (150 µm)

- Saw kerfs must be at least 25 µm and into the dicing tape (through the entire wafer thickness)
- Die attach materials can be non-conductive or conductive pastes, die attach films (DAF) and solder preforms; other processes can be discussed per customer requirements

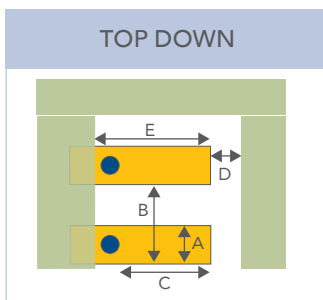
LOW PROFILE & FINE PITCH WIRE BOND

Plating and layout requirements for substrate pad design as well as wire parameters:

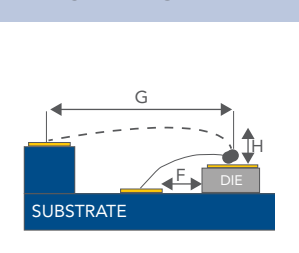
- Wedge Bond - ENIG plating is acceptable; typical wire types include Al, Au and Pt
- Ball Bond - ENEPIG plating is recommended; typical wire types include Au & Cu

Processes that use Au ball bond, require Gold plate per MIL-G-45204, Type III, Grade A, Class 1:

- 99.9% purity minimum
- < 90 Knoop hardness
- 50 µ" thick, minimum



SIDE PROFILE



TYPICAL WIRE BOND SPECIFICATIONS

	DESCRIPTION	ORGANIC (min)	CERAMIC (min)
A	Wire bond Pad	0.004" (100 µm)	0.003" (75 µm)
B	Wire bond Pad Pitch	0.008" (200 µm)	0.006" (150 µm)
C	Overlap of Wire bond Lead Edge to Via	0.008" (200 µm)	0.007" (175 µm)
D	Space Solder Mask to Wire bond Lead Edge	0.004" (100 µm)	-
E	Overlap of Wire bond Lead Edge to Solder Mask	0.008" (200 µm)	-
F	Space of Die Edge to Wire bond Lead Edge (assumes no ground plane for die attach)	0.015" (375 µm) or 2x Die Thickness (whichever is greater)	
G	Maximum Wire Length	0.250" (6350 µm)	
H	Maximum Wire Height	0.100" (2540 µm)	

NOTE

These dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

FLIP CHIP & UNDERFILL

Package Size (approximate):

- Min: 10 mm x 10 mm
- Max: 63 mm x 63 mm

Flux:

- No-clean fluxes
- Water-soluble fluxes
- RMA-based fluxes

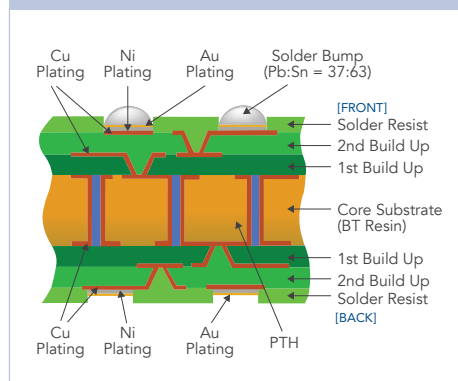
Substrate BGA Solder Ball:

- Min Size: 0.18" dia (approx.)
- Max Size: 0.025" dia (approx.)
- Material: Eutectic Pb:Sn (37:63) or Pb-Free

Substrate BGA Pad:

- Shortest BGA Ball Pitch: 0.80 mm x 0.80 mm
- Furthest Pitch:
No constraint
- Pad Layout: Any configuration is acceptable

SUBSTRATE STRUCTURE (TYPICAL)



LAYER THICKNESS (TYPICAL)

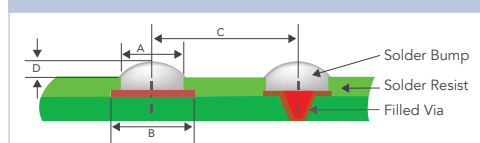
LOCATION	STANDARD (μm)	CUSTOM (μm)
Core Substrate	800	400*
Core Cu	25	21
Build-up Cu	14.5	2
Insulation Layer	33	12
Solder Resist Layer	21	18
Nickel Plating	3 - 7	
Gold Plating	0.03 ~ 0.12	

No. of Build Up Layers: 1, 2, 3, 4 / side;
No. of Core Layers: 2, 4; *Coreless also available

LAYER THICKNESS (TYPICAL)

	ITEM	STANDARD	CUSTOM
A	Flip Chip Pad Diameter (Solder Resist Opening)	100 μm	75 μm
B	Flip Chip Pad Metal Land Dia.	145 μm	100 μm
C	Flip Chip Pad Pitch	225 μm	130 μm
D	Solder Bump Height	32 μm ± 5 μm	

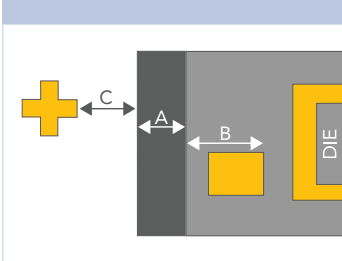
FLIP CHIP PAD DESIGN RULE



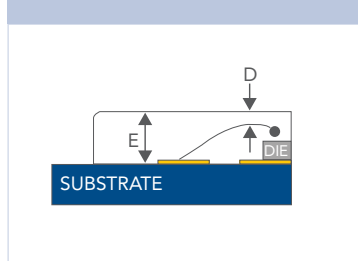
ENCAPSULATION

- Maximum encapsulation thickness (board surface to top of encapsulation): 0.024" (600)
- Automated dispense tool heated work area: 12" x 16"
- Total work area: 20" x 30"
- Machine positioning accuracy and repeatability: +/- 0.001"

TOP DOWN



SIDE PROFILE



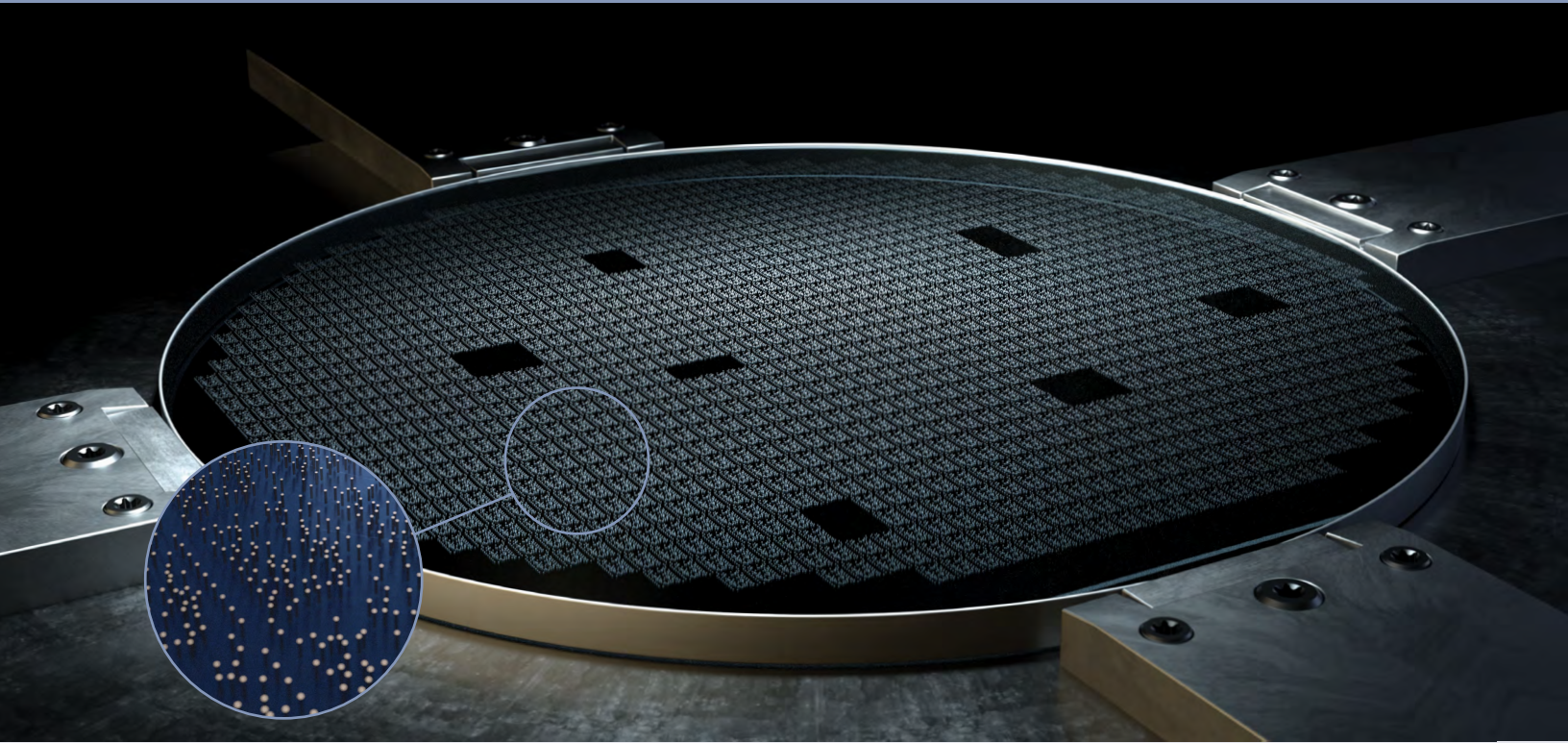
TYPICAL PACKAGE DESIGN RULES

	DESCRIPTION	ORGANIC (min) INCHES (μm)
A	Dam Width	0.012" (300)
B	Space of Dam to Wire bond Lead Edge	0.012" (300)
C	Space of Fiducial to Dam*	0.007" (175)
D	Overlap of Encapsulation to Top of Wire bond Loop	0.007" (175)
E	Height of Encapsulation**	= A / 2

*Must be outside encapsulated region
**Board surface to top of encapsulation

GLASS CORE TECHNOLOGY

ULTRA-MINIATURIZED | HIGHLY INTEGRATED | HIGH PERFORMANCE



Through-Glass Vias (TGVs) in Glass Substrates

The industry's only proven process for metalization and hermetic sealing of ultra-high-density Through-Glass Vias (TGVs) enables:

Extreme Miniaturization & Integration

High Performance Electronics

High Reliability Packaging Solutions

Redistribution Layer (RDL) Circuit Patterning on Glass

RDL's unique thin-film process enables circuit formation on glass substrates, providing for:

Low Loss Fan-Out of Chip and Package Interconnects

Lower Cost Compared to Traditional Silicon-Based Interposers

Channels and Shaped Vias in Glass Substrates

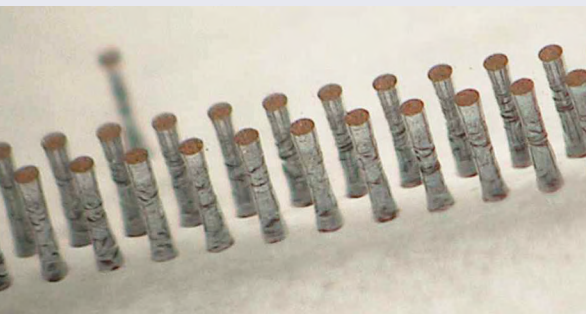
Glass is ideal for applications requiring shaped vias and channels, including:

Microfluidic & Fluidic Devices

3D Structures

Integrated Passive Devices, Filters

Endless IoT Applications



HIGH PERFORMANCE ELECTRONICS

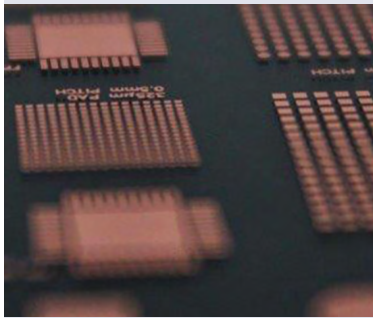
DESIRED PROPERTIES		GLASS	SILICON	ORGANIC LAMINATE
Total Thickness Variation (TTV)	< 5 μm			
Warp	< 2 μm / 20 mm			
Insulation Resistance	High			
Optical Transparency	Optical I/O			
Surface Roughness	< 5 nm			
Coefficient of Thermal Expansion (CTE)	3.2 ppm / C			
Hermetic Vias	Mil-Spec.			

Glass substrates offer high structural integrity, resistance to vibration and temperature, environmental ruggedness, and low electrical loss, making them ideal for next generation microelectronics demands.

Samtec's proprietary **Glass Core Technology** process leverages the performance benefits of glass to enable *performance optimized, ultra-miniaturized substrates for next generation designs.*

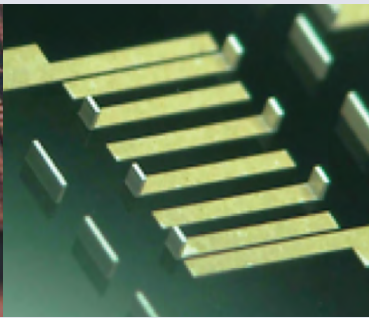
SEE PAGES 10-11 FOR TYPICAL DESIGN GUIDELINES.

GLASS CORE TECHNOLOGY PRACTICAL APPLICATIONS



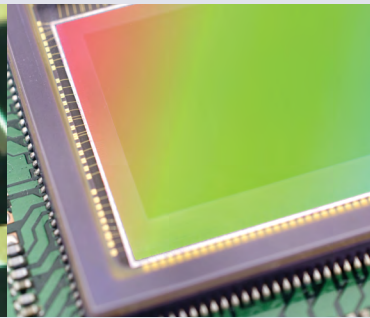
Automotive MEMS
and Sensors

Smart Building
Sensor Modules



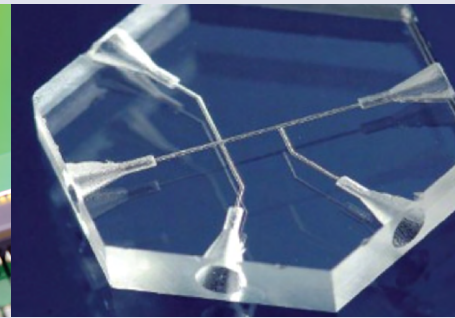
RF Components and Modules

Advanced RF SiP
Automotive RF



CMOS Image Sensor (CIS)

Automotive Camera Modules
Active Imaging & LiDAR



Microfluidics & Lab-on-Chip

Solid State Medical Imaging
Medical Robotics Sensors

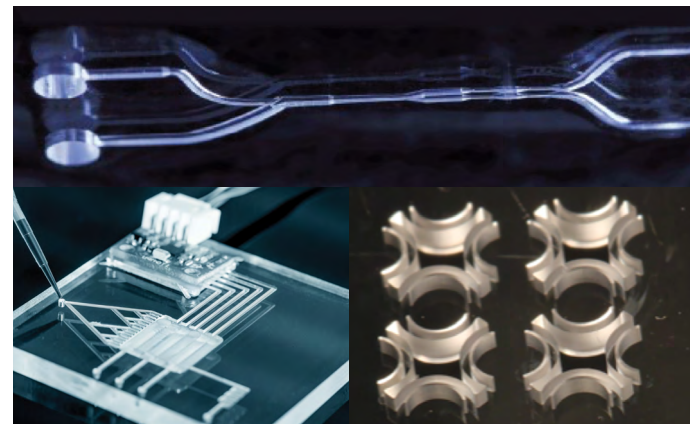
GLASS CORE TECHNOLOGY | ROADMAP

With a wide market reach and broad range of flow speeds, fused silica-based substrates are an ideal solution for microfluidic devices, a growing market sector within the biomedical industry. Applications include:

- Fluidic structures for electronics cooling designs
- Microfluidic structures for biomedical devices and lab-on-chip application designs

Microstructuring possibilities also include formation of microchannels, cavities, larger cooling channels, mixing channels, 180-degree bends, as well as ferrule openings for optical fibers and v-grooves, among others.

Contact the specialists at Samtec Microelectronics to discuss solutions for your next generation system design.



GLASS CORE TECHNOLOGY DESIGN GUIDELINES

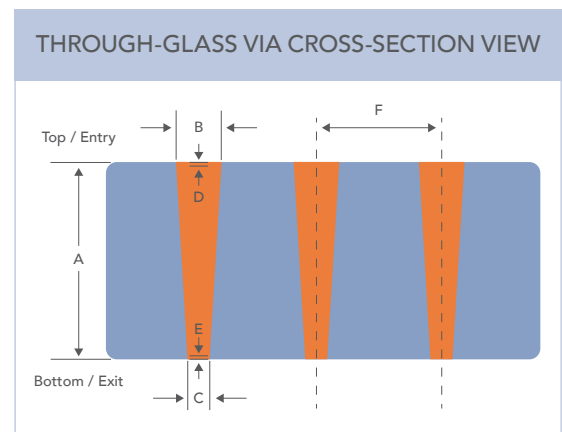
THROUGH-GLASS VIA (TGV) ENABLED GLASS INTERPOSERS

Samtec's Through-Glass Vias (TGVs) enable Glass Core Technology (i.e., glass interposers, smart glass substrates and microstructured glass substrates). TGV-enabled glass substrates permit the integration of glass and metal into a single wafer, while interposers promote more efficient package interconnects and manufacturing cycle times. The hermetically sealed TGVs are manufactured from both high quality borosilicate glass, fused silica (aka quartz), and sapphire.

Through the use of high quality glass wafer material, combined with advanced interconnect technologies (e.g., Redistribution Layer), Samtec's Glass Core Technology enables a one-of-a-kind packaging product.

STANDARD TGV DESIGN GUIDELINES						
	DETAIL	BOROSILICATE GLASS			FUSED SILICA	
		Units (μm)			Units (μm)	
A	Nominal Glass Thickness*	200	300	500	300	500
B	Top Via Diameter	40 $\pm$ 5	60 $\pm$ 5	70 $\pm$ 5	55 $\pm$ 5	70 $\pm$ 5
C	Bottom Via Diameter	40 $\pm$ 5	60 $\pm$ 5	70 $\pm$ 5	55 $\pm$ 5	65 $\pm$ 5
D	Top Via Depth	< 0.5			< 0.5	
E	Bottom Via Depth	< 0.5			< 0.5	
F	Via Pitch	2x B			150	
	Total Thickness Variation (TTV)	5			5	
	Via Positional Accuracy	$\pm$ 13			$\pm$ 5	
	Slot Width				70 $\pm$ 5	
	Slot Length (Demonstrated)				1000	

*Custom nominal thicknesses also available.



BOROSILICATE GLASS	
CHARACTERISTICS:	APPLICATIONS:
• Excellent clarity and rigidity • High thermal shock resistance • Low density glass • Low & high thermal expansion	• Biomedical • 2.5D / 3D Packaging • Displays • Optoelectronics

FUSED SILICA	
CHARACTERISTICS:	APPLICATIONS:
• High purity material • Low dielectric constant and loss factor • Very low thermal expansion • Wide operating temp range	• Biomedical • Microfluidics & Lab-on-a-Chip • RF MEMS • Optics, Imaging & Photonics

NOTE

These dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

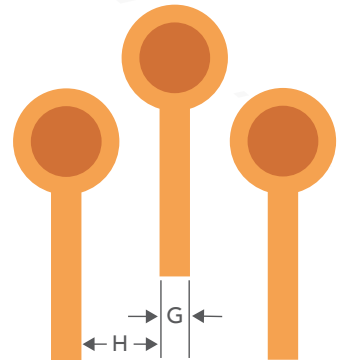
REDISTRIBUTION LAYER (RDL) TECHNOLOGY

RDL provides a unique thin-film approach for interfacing to TGVs. The technique enables circuit formation on various glass substrates.

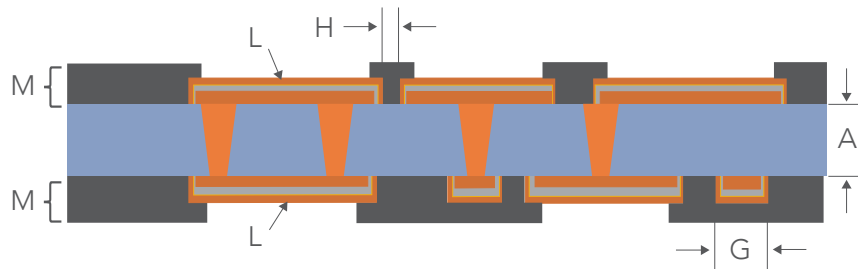
GLASS CORE TECHNOLOGY CAPABILITIES

	SPECIFICATIONS	CURRENT	ROADMAP
	No. of Metal Layers per Side	2	4
A	Glass Core Thickness	300 to 700 μm	100 μm
	Core Via Diameter	40 μm	10 μm
	Core Via Pitch	100 μm	40 μm
G, H	Line / Spacing	15 μm / 15 μm	5 μm / 5 μm
L	Copper Thickness	1-10 μm	
M	Polyimide Thickness 1 & 2	5 μm	
	Solder Ball Types	Sn63Pb37, PbSn5, PbSn10, SAC	Cn / Sn Pillars
	Under Bump Metalization (UBM)	ENIG	

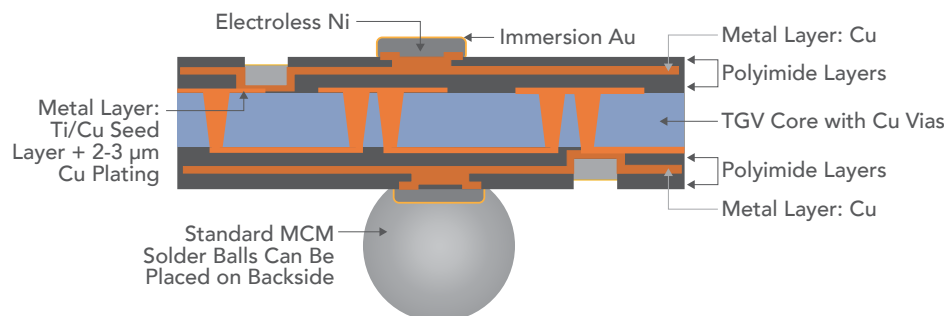
TOP VIEW OF CIRCUIT FOR TOP / BOTTOM RDL



CROSS SECTION - 2 METAL LAYERS (CURRENT CAPABILITY)



CROSS SECTION - 4 METAL LAYERS (FUTURE CAPABILITY)



MICROELECTRONICS SYSTEM SUPPORT

FULL CHANNEL CHALLENGES

MINIATURIZATION AND INTEGRATION

IC PACKAGE, PCB ROUTING AND BREAKOUT REGIONS

MATERIALS SELECTION

PROTOCOL COMPLIANCE

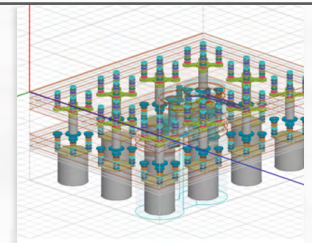
COST CONTROL

POWER AND THERMAL MANAGEMENT

FULL CHANNEL EXPERTISE & SUPPORT

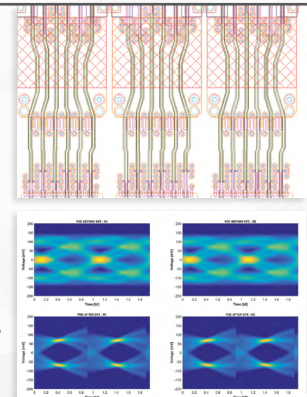
PACKAGE AND PCB DESIGN

- Bumpout / ballout optimization
- Ballout transition structures
- Layout & routing
- Materials recommendations



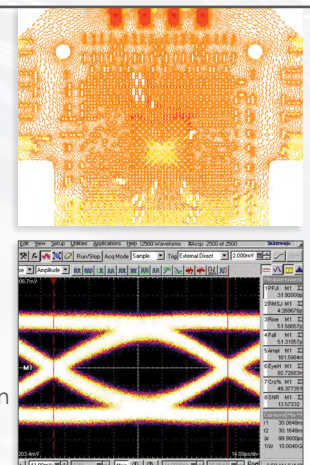
MODELING AND SIMULATION

- Validate implementation and signaling requirements for critical channels
- High bandwidth full-wave simulations
- Design rules for package and PCB designs
- Simulations via High-Performance Computing (HPC)



ANALYSIS, TESTING & VALIDATION

- Characterization at frequencies to 67 GHz and beyond
- Package, PCB and system-level Signal Integrity / Power Integrity
- Material characterization
- Post-design test, simulation and measurement
- Measurement of test structures for Signal / Power Integrity optimization



Support and services are available at any level required: from early stages of the design process including package design, material selection and PCB routing, through in-depth analysis, modeling and simulation, with measurement validation services available to 67 GHz, **Samtec Teraspeed Consulting and Signal Integrity Group engineers help optimize and validate high-performance systems.**

SILICON-TO-SILICON SUPPORT | EVERY POINT OF INTERCONNECTION IS CRITICAL



CONTACT OUR
SIGNAL INTEGRITY
ENGINEERS



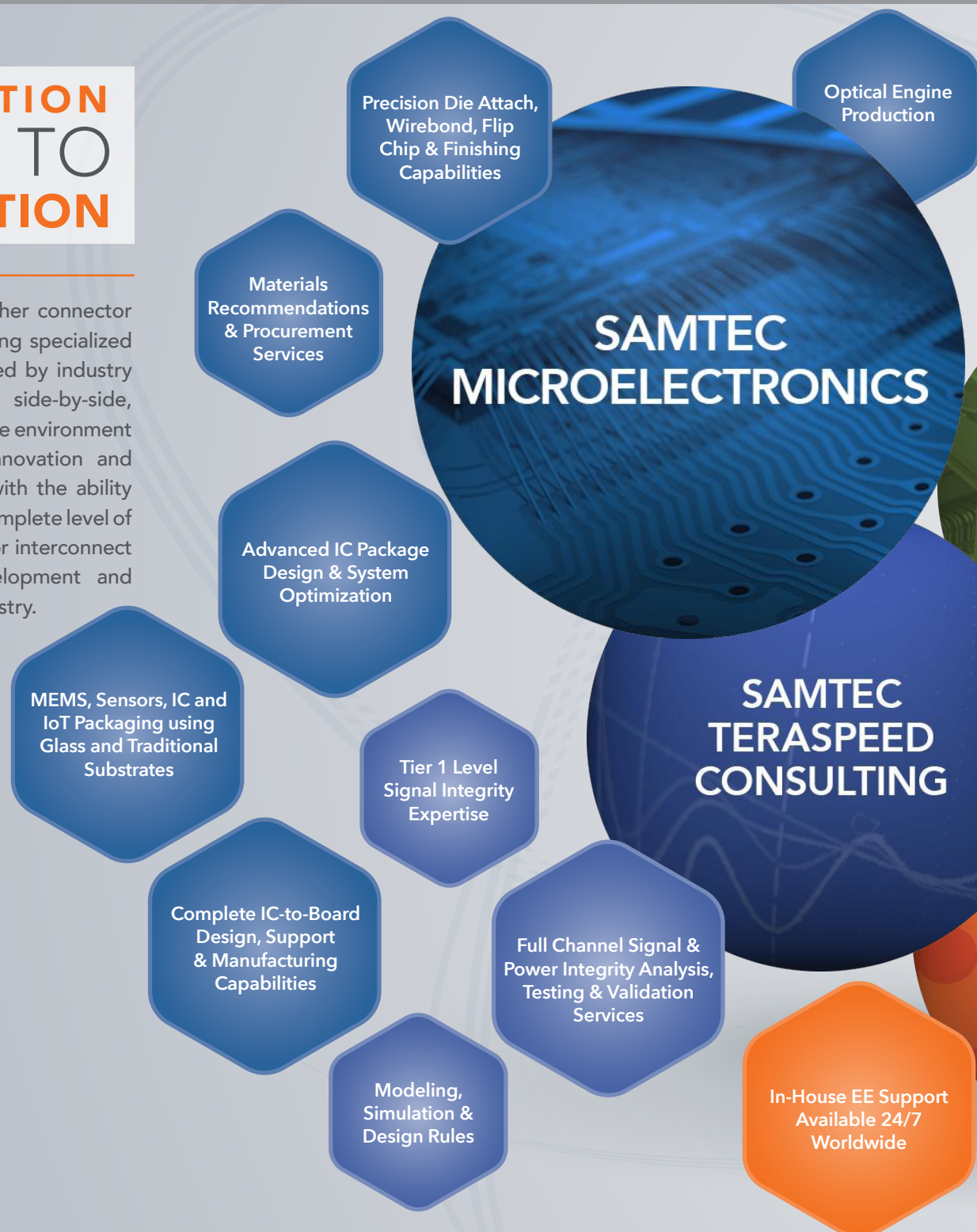
sig@samtec.com
+1-812-981-8398
+1-812-944-6733

TECHNOLOGY CENTERS

ENABLING COMPLETE SYSTEM OPTIMIZATION FROM SILICON-TO-SILICON

INTEGRATION LEADS TO INNOVATION

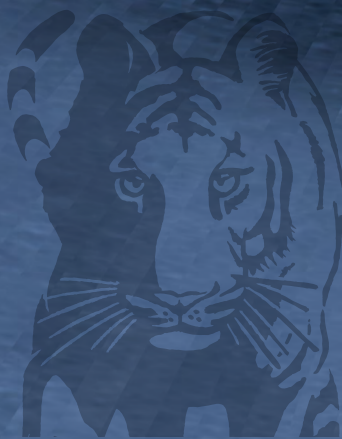
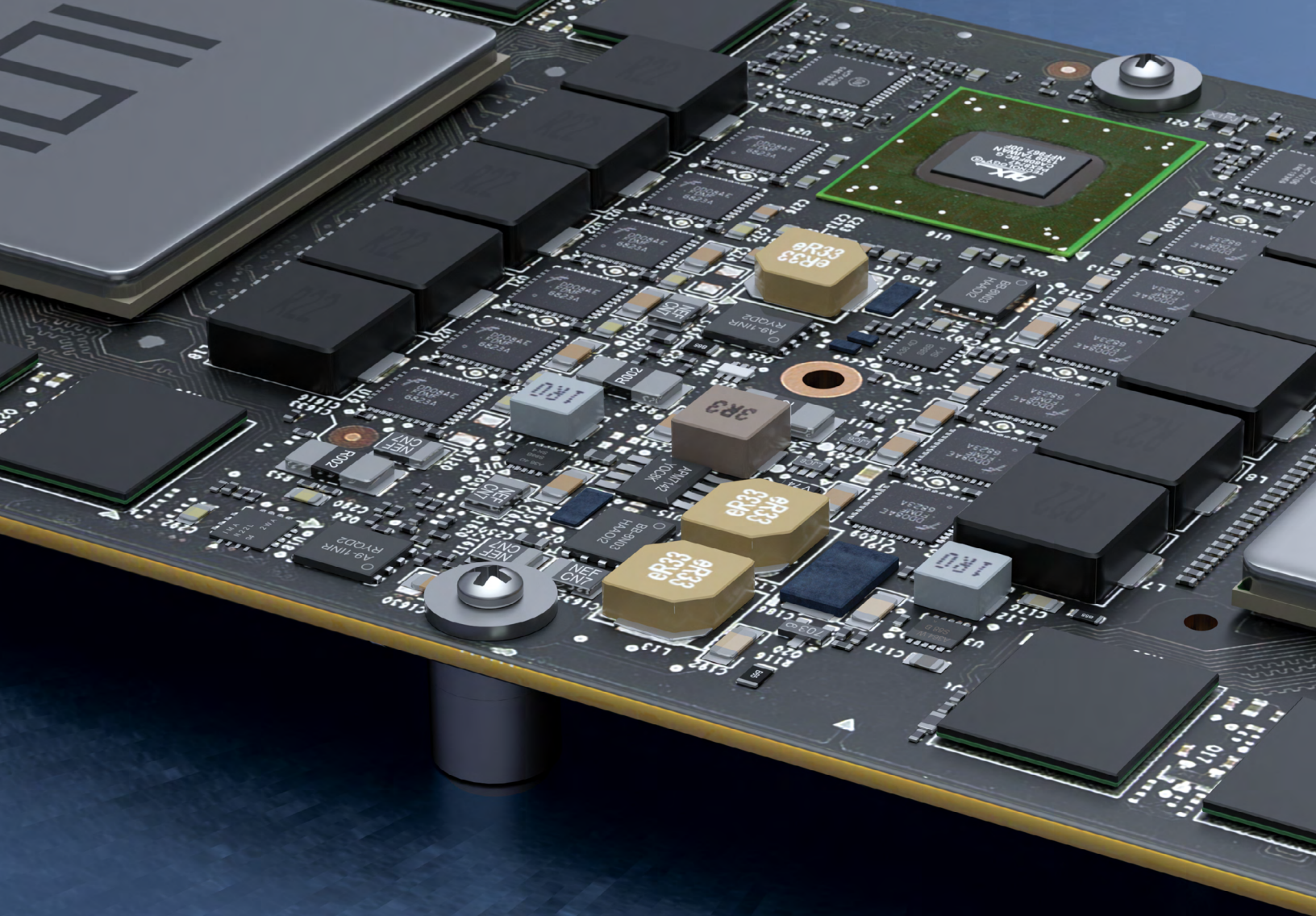
Samtec isn't just another connector company. By integrating specialized Technology Centers led by industry experts working side-by-side, Samtec fosters a unique environment conducive to true innovation and collaboration, along with the ability to provide the most complete level of service and support for interconnect system design, development and production in the industry.





For more information,
please visit:

[www.samtec.com/
tech-centers](http://www.samtec.com/tech-centers)



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AUGUST 2017