ANP-41

Powering the Zynq-7000 All Programmable SoC with XRP7714

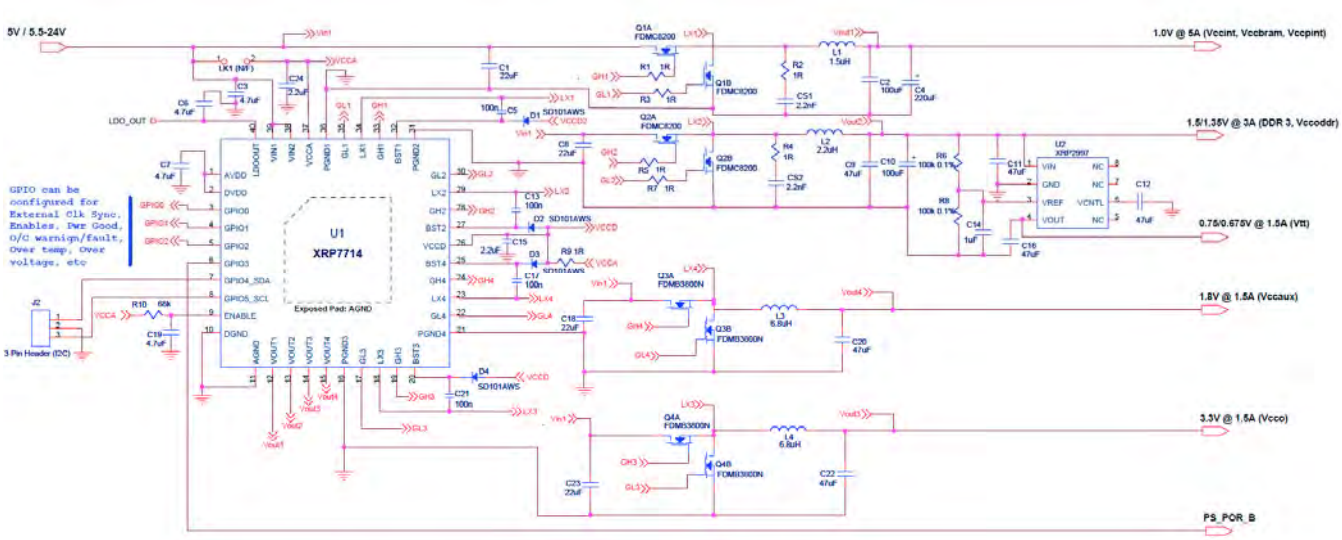
May 2013 Rev. 1.0.1

GENERAL DESCRIPTION

This reference design is a complete four output power system designed to power a Xilinx Zynq-7000 All Programmable (AP) SoC and associated DDR3 memory. This design was developed and validated on a customer board by our applications engineering team. The power system provides 1.0V, 1.5V, 0.75V, 1.8V, and 3.3V in 1.5 square inch solution. The order and ramp rates for each supply are programmed to accommodate Zynq-7000 AP SoC sequencing requirements. All power supply operations can be controlled over an I^2C interface. Faults, output voltages and currents can also be monitored. Four GPIO signals are available and can be programmed to provide the status of power good signals, enables, and faults. Unused GPIO pins can be programmed for use as I/O expansion. The board is supported by PowerArchitect™ 4.x and connects to the Exar Communications Module (XRP77XXEVB-XCM).

FEATURES

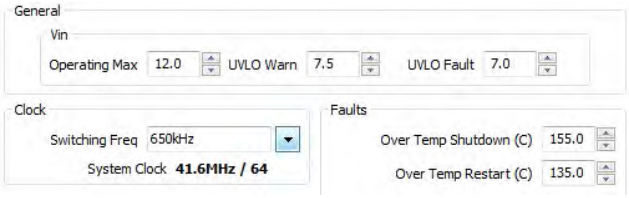
- **Xilinx Zynq-7000 All Programmable SoC Power System**
  - 4 Channel Power System using XRP7714 Programmable Digital PWM Switching Controller
- **Validated in actual end system**
- **I^2C Interface**
  - Programming
  - Monitoring
  - Control



ZYNQ-7000 AP SOC POWER SOLUTION

The Zynq-7000 AP SoC power reference design provides 4 output voltages regulated down from a 12V supply. The order and ramp rates for each output are programmed to accommodate Zynq-7000 AP SoC sequencing requirements.

The power system was designed to operate at 650kHz as a good trade-off between space and efficiency.



Output 1 / Channel 1 Configuration

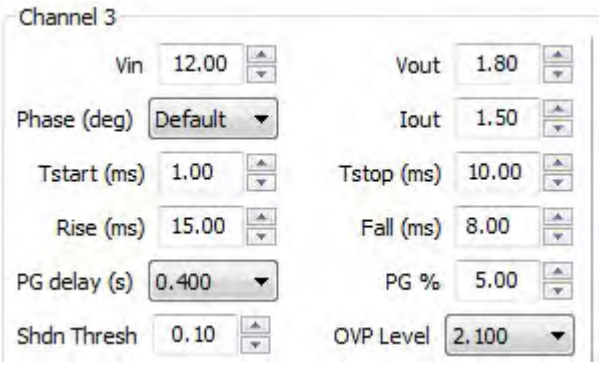
Channel 1 is designed to provide 1V to VCCINT, VCCBRAM and VCCPINT Zynq-7000 AP SoC rails at 5A.

Output 2 / Channel 2 Configuration

Channel 2 provides 1.5V to the DDR3 SDRAM subsystem as well as the DDR3 block inside the Zynq-7000 AP SoC. In addition, it sources the XRP2997 DDR Bus Termination Regulator which provides termination voltage for the DDR3 SDRAM signals. The channel is designed to support a 3A load.

Output 3 / Channel 3 Configuration

Channel 3 is designed to provide 1.8V to VCCAUX and VCCPLL Zynq-7000 AP SoC rails at 1.5A.



Output 4 / Channel 4 Configuration

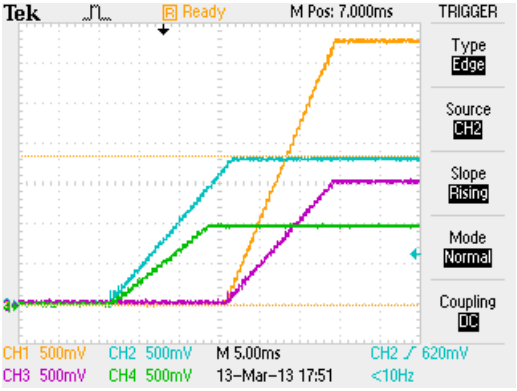
Channel 4 provides 3.3V to Zynq-7000 AP SoC IO banks (VCCO) and peripherals in the system. It is designed to support a 1.5A load.

CHANNEL SEQUENCING

The XRP7714 has been programmed to meet the Zynq-7000 AP SoC power up sequencing requirements.

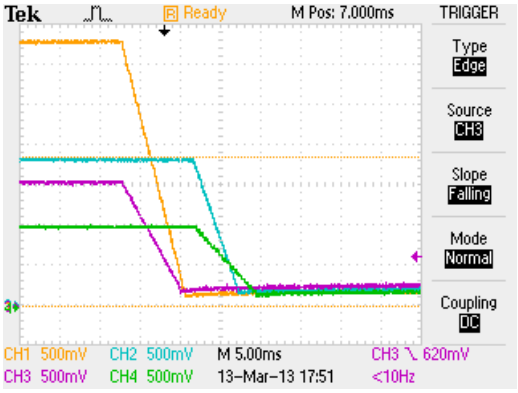
Power-On Sequencing

1. **1.0V** supply with 0.077V/msec ramp rate
2. **1.8V** supply with 0.12V/msec ramp rate
3. **1.5V and 3.3V supplies** - the 1.5V supply with 0.115V/msec ramp rate reaching the target level at the same time as the 3.3V supply with 0.254V/msec ramp rate.



Power-Down Sequencing

1. **1.5V and 3.3V supplies** – the 1.5V supply following 0.1875V/msec ramp down rate; the 3.3V supply following 0.4125V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.
2. **1.0V and 1.8V supplies** – the 1.0V supply following 0.125V/msec ramp down rate; the 1.8V supply following 0.225V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.



ZYNQ-7000 AP SOC POWER ON RESET

XRP7714 will generate a power on reset signal on GPIO3 to the Zynq-7000 AP SoC 400ms after the last rail is in regulation.

I²C INTERFACE

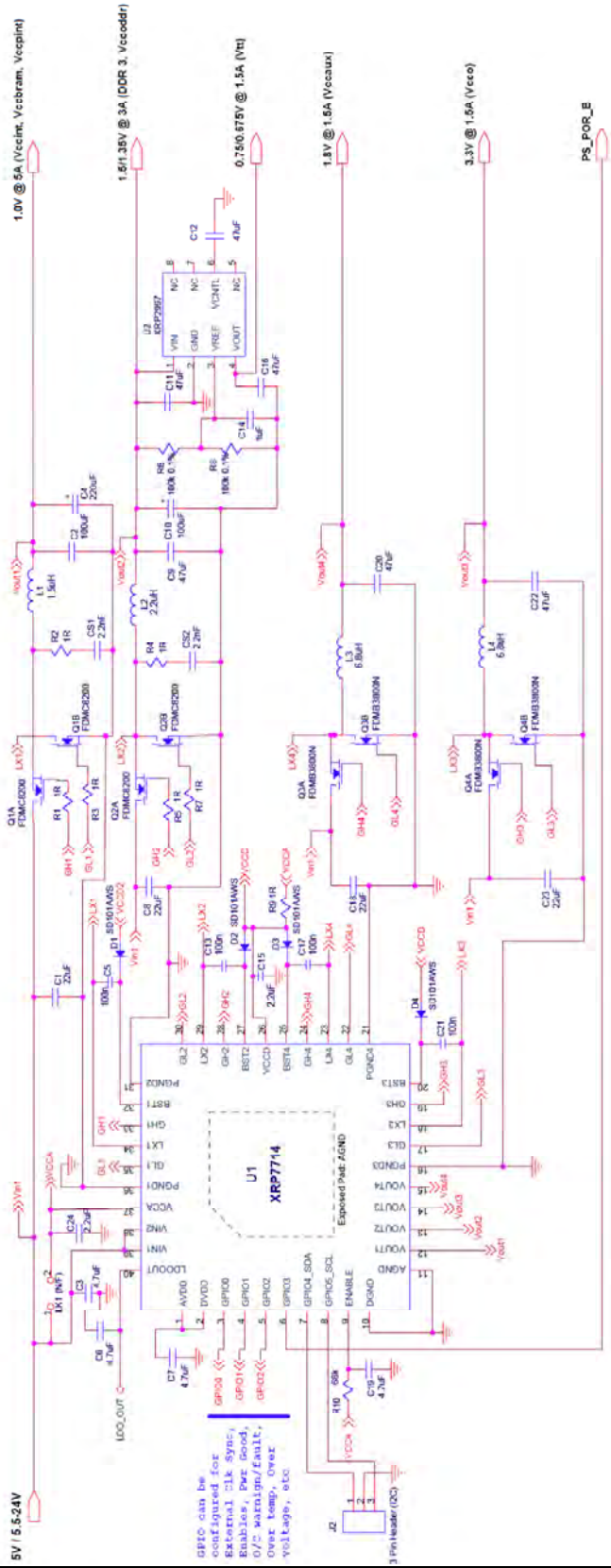
The Zynq-7000 AP SoC power reference design schematic has an I²C interface connector (J1) to connect to the Exar Communications Module (XRP77XXEVB-XCM) to interface with PowerArchitect™ during the development phase and to Zynq-7000 AP SoC I²C port for control and monitoring of the power subsystem in the final product.

For more information how to implement power subsystem control and monitoring via I²C bus refer to ANP-31.

I²C pull-up resistors are not included in this design. The Zynq-7000 AP SoC system board must have these installed if communication between Zynq-7000 AP SoC and XRP7714 is desired.

The pull-up resistors are not required when communicating with the XCM module which has pull-up resistors installed (check jumper settings).

SCHEMATICS


1.0V @ 5A (Vccint, Vccbram, Vccpint)
1.5/1.35V @ 3A (DDR 3, Vcceddr)
0.75/0.675V @ 1.5A (Vtt)
1.8V @ 1.5A (Vccaux)
3.3V @ 1.5A (Vcco)
PS_POR_B
5V / 5.5-24V
U1
XRP7714
Exposed Pad: AGND
GPIO can be configured for External clk sync, Enables, Pwr Good, O/C warning/fault, Over temp, Over voltage, etc

BILL OF MATERIAL

Ref.	Qty	Manufacturer	Part Number	Size	Component
U1	1	EXAR	XRP7714ILB-F	40-TQFN	XRP7714 PWM Step-Down DC/DC Controller
U2	1	EXAR	XRP2997	8-SOIC	2A DDR I/II/III Bus Termination Regulator
Q1,Q2	1	Fairchild	FDMC8200	Power 33	Dual N-Channel PowerTrench MOSFET 30V, 9.5mOhm & 20mOhm
Q3,Q4	3	Fairchild	FDMB3800N	MicroFET 3x1.9	Dual N-Channel PowerTrench MOSFET 30V, 4.8A, 40mOhm
D1,D2,D3,D4	4	Vishay	SD101AWS-V-GS08	SOD323	Small Signal Schottky Diode 60V, 30mA
L1	1	Wurth Elektronik	7440650015		Inductor 1.5uH, 16.6mOhm, 9A
L2	1	Wurth Elektronik	744774022		Inductor 2.2uH, 20mOhm, 6.5A
L3, L4	2	Wurth Elektronik	7447715006		Inductor 6.8uH, 40mOhm, 3A
C1,C8,C18,C23	4	Murata	GRM32ER71E226KE15L	1210	Capacitor Ceramic 22uF, 25V, X7R
C2	1	Murata	GRM32ER60J107ME20L	1210	Capacitor Ceramic 100uF, 6.3V, X5R
C3,C6,C7,C19	4	Murata	GRM21BR71C475KA73	0805	Capacitor Ceramic 4.7uF, 16V, X7R
C4	1	SANYO/Panasonic	EEF-SX0E221R		Capacitor POSCAP, 220uF
C5,C13,C17,C21	4	Murata	GRM188R71H104KA93D	0603	Capacitor Ceramic 0.1uF, 50V, X7R
C9,C11,C12,C16,C20,C22	6	Murata	GRM32ER71A476KE15L	1210	Capacitor Ceramic, 47uF, 10V, X7R
C10	1	SANYO/Panasonic	EEF-SX0G101R		Capacitor POSCAP, 100uF
C14	1	Murata	GRM21BR71H105KA12L	0805	Capacitor Ceramic, 1uF, 50V, X7R
C15,C24	2	Murata	GRM21BR71C225KA12L	0805	Capacitor Ceramic 2.2uF, 16V, X7R
CS1, CS2	2	Murata	GRM188R71H222KA01D	0603	Capacitor Ceramic 2200pF, 50V, X7R
R1,R2,R3,R4,R5,R7,R9	7	Vishay/Dale	CRCW06031R00FKEA	0603	Chip Resistor 1 Ohm, 1%, 1/10W
R6,R8	2	Vishay/Dale	TNPU0603100KBZEN00	0603	Chip Resistor 100K Ohm, 1/10w, 0.1%
R10		Vishay/Dale	CRCW060368K0FKEA	0603	Chip Resistor 68K Ohm, 1/10w, 1%
J1	1	Wurth Elektronik	61304011121	HDR1X2	Connector Header 2 Positions 0.1” Vertical Gold

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	04/09/2013	Initial release of document
1.0.1	05/08/2013	Changed the document name

FOR FURTHER ASSISTANCE

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